

Project Name : NH14CU

Platform : Ivy Bridge(PROCESSOR)+Panther Point(PCH)

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30. CPU CORE (OZ8293)

31. CPU VCCSA

32. +1.05V(OZ8116)/+0.75VS/+1.8V

33. +1.5VS/+5VA (OZ8153)

34. BATT IN/CHARGER(OZ8602)

35. iGPU Core(OZ8293)

36. TP/LED/WEBCAM/USB CHARGER/RS-232 CON

37. VCC SW/+3.3VA/HIGH-SPEED CAP

38. USB 3.0

39. Reseved

40. History

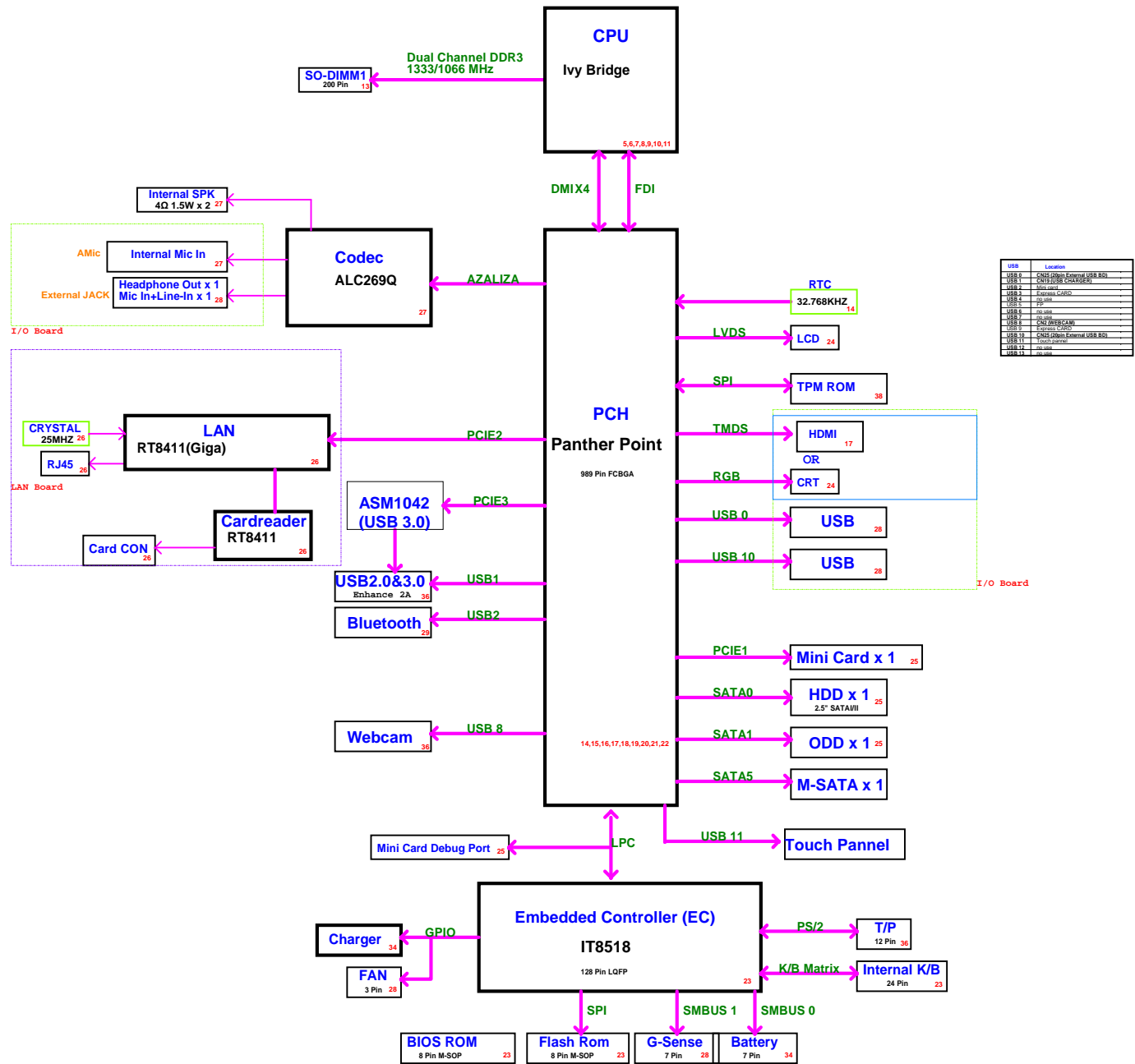
M/B Schematic Version Change List

| Release Date | Version | PCB P/N | PCB Description | PCBA P/N | Note |
|--------------|---------|---------|-----------------|----------|------|
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Daughter Board Schematic Version Change List

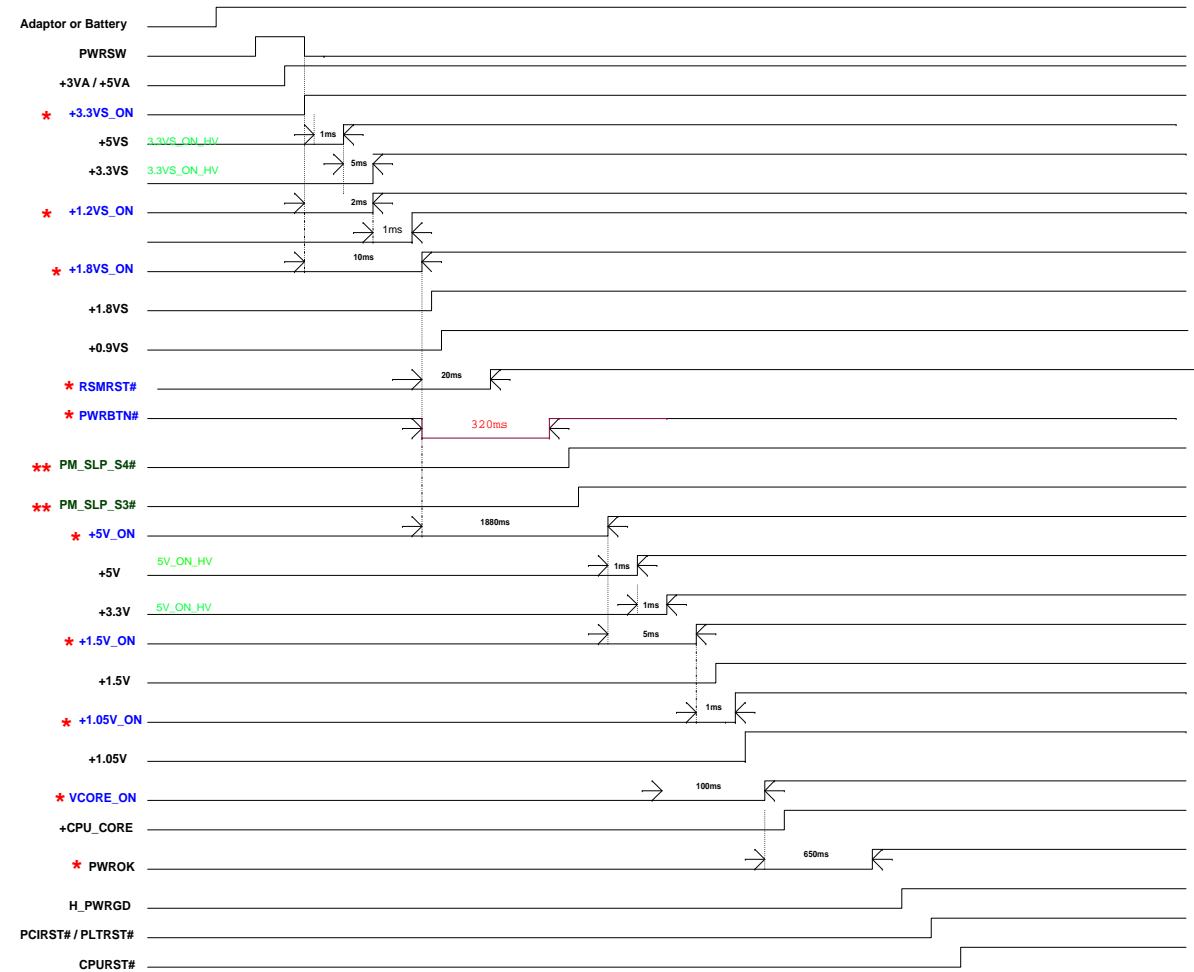
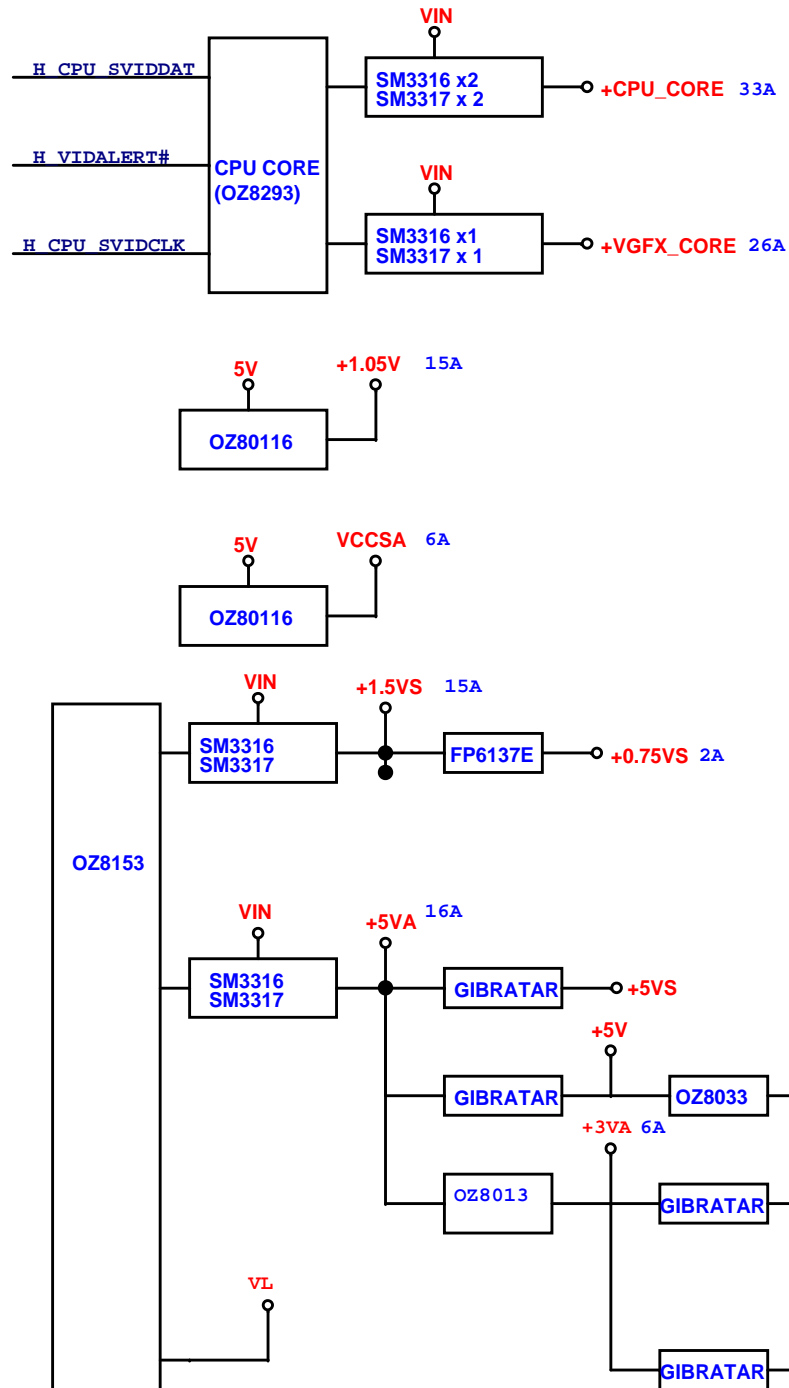
| Release Date | Version | PCB P/N | PCB Description | PCBA P/N | Note |
|--------------|---------|---------|-----------------|----------|------|
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SYSTEM BLOCK DIAGRAM



POWER BLOCK DIAGRAM

System Poewr On Sequence



* EC Control Pin (O/P)
** EC Control Pin(I/P)

| Panther Point GPIO | |
|-----------------------|--------------------|
| GPIO0 | PM_BM_BUSY# |
| GPIO1 | EC_EXTSMI# |
| GPIO2 | INT_PIRQ# |
| GPIO3 | INT_PIRQ# |
| GPIO4 | INT_PIRQ# |
| GPIO5 | INT_PIRQ# |
| GPIO6 | BIOS_REC |
| GPIO7 | N.C(TACH3) |
| GPIO8 | N.C |
| GPIO9 | N.C(WOL_EN) |
| GPIO10 | N.C(ALERT#) |
| GPIO11 | SMB_ALERT# |
| GPIO12 | LAN_PHYPC |
| GPIO13 | N.C(GLAN_DOCK#) |
| GPIO14 | N.C(NETDETECT) |
| GPIO15 | PM_STPPCI# |
| GPIO17 | N.C(TACH0) |
| GPIO18 | N.C |
| GPIO19 | SATA1GP |
| GPIO21 | SATA0GP |
| GPIO22 | N.C(SCLOCK) |
| GPIO23 | LDRQ1# |
| GPIO24 | CRB_SV_DET |
| GPIO25 | PM_STPCPU# |
| GPIO26 | PM_SLP_S4_STATE# |
| GPIO27 | QRT_STATE0 |
| GPIO28 | QRT_STATE1 |
| GPIO29 | USB_OC#5 |
| GPIO30 | USB_OC#6 |
| GPIO31 | USB_OC#7 |
| GPIO32 | PM_CLKRUN# |
| GPIO33 | HDA_DOCK_EN |
| GPIO34 | N.C(HDA_DOCK_RST#) |
| GPIO35 | CLK_SATA_OE# |
| GPIO36 | SATA2GP |
| GPIO37 | SATA3GP |
| GPIO38 | ODD_DET |
| GPIO39 | ICH_GPIO39 |
| GPIO40 | USB_OC#1 |
| GPIO41 | USB_OC#2 |
| GPIO42 | USB_OC#3 |
| GPIO43 | USB_OC#4 |
| GPIO48 | MFG_MODE |
| GPIO49 | H_PWRGD |
| GPIO50 | PCI_REQ#1 |
| GPIO51 | PCI_GNT#1 |
| GPIO52 | PCI_REQ#2 |
| GPIO53 | PCI_GNT#2 |
| GPIO54 | PCI_REQ#3 |
| GPIO55 | PCI_GNT#3 |

| ITE8518 GPIO | | Default Pull/Mode |
|-----------------|------------------|----------------------|
| GPA0 | PID_3_RF_LED_ON# | UP / GPI |
| GPA1 | BATT_VA_OFF# | UP / GPI |
| GPA2 | BT_L_BEEP | UP / GPI |
| GPA3 | WLAN_PWR# | UP / GPI |
| GPA4 | +1.05V_ON | UP / GPI |
| GPA5 | SENBAT_V | UP / GPI |
| GPA6 | PM_RSMRST# | UP / GPI |
| GPA7 | EC_BL_PWM | UP / GPI |
| GPB0 | PM_SLP_S4# | UP / GPI |
| GPB1 | PM_SLP_S3# | UP / GPI |
| GPB2 | 3G_PWR# | Dn / GPI |
| GPB3 | SMBCLK | / GPI |
| GPB4 | SMBDAT | / GPI |
| GPB5 | H_A20GATE | / GPO |
| GPB6 | H_RCIN# | UP / Func1 |
| GPB7 | SAFTY_PROTECT | Dn / GPI |
| GPC0 | +1.5V_ON | Dn / GPI |
| GPC1 | SMB_CLK_EC | / GPI |
| GPC2 | SMB_DAT_EC | / GPI |
| GPC3 | PID_0_CHG_B_LED | Dn / GPI |
| GPC4 | PWRBTN3# | Dn / GPI |
| GPC5 | PANEL_DETECT_2 | Dn / GPI |
| GPC6 | VCCSA_ON | Dn / GPI |
| GPC7 | +1.5VS_ON | UP / GPI |
| GPD0 | ADAP_IN | UP / GPI |
| GPD1 | PWRBTN# | UP / GPI |
| GPD2 | PLT_RST# | UP / Func1 |
| GPD3 | PM_SUS_STAT# | UP / GPI |
| GPD4 | EC_EXTSMI# | UP / GPI |
| GPD5 | Fastcharge_EN | UP / GPI |
| GPD6 | +5V_ON | Dn / GPI |
| GPD7 | SET_V | Dn / GPI |
| GPE0 | LID# | Dn / GPI |
| GPE1 | PWR_USB_LED | Dn / GPI |
| GPE2 | ALL_SYS_PGD | Dn / GPI |
| GPE3 | Vcore_ON | Dn / GPI |
| GPE4 | PWRSW | UP / GPI |
| GPE5 | LVDS_VIN | Dn / GPI |
| GPE6 | WLAN_ON | Dn / GPI |
| GPE7 | AMP_MUTE# | UP / GPI |
| GPF0 | PCH_BL_EN | UP / GPI |
| GPF1 | +1.8V_ON | UP / GPI |
| GPF2 | BT_ON | UP / GPI |
| GPF3 | N.C | UP / GPI |
| GPF4 | TP_CLK | UP / GPI |
| GPF5 | TP_DATA | UP / GPI |
| GPF6 | EC PECl | UP / GPI |
| GPF7 | CHG_HI_VOLT# | UP / GPI |
| GPG0 | PWRBTN2# | Dn/GPO/TM |
| GPG1 | +3.3VS_ON | Dn/GPO/ID7 |
| GPG2 | EC PORST | |
| GPG6 | WEBCAN_ON | Dn / GPI |
| GPH0 | PM_CLKRUN# | Dn/GPI/ID0 |
| GPH1 | PID_1_CHG_R_LED | Dn/GPI/ID1 |
| GPH2 | PID_2_PWR_LED | Dn/GPI/ID2 |
| GPH3 | EC_HSCS0# | Dn/GPI/ID3 |
| GPH4 | EC_HSCK | Dn/GPI/ID4 |
| GPH5 | EC_HMISO | Dn/GPI/ID5 |
| GPH6 | EC_HMOSI | Dn/GPI/ID6 |

| ITE8518 GPIO | | Default Pull/Mode |
|-----------------|--------------|----------------------|
| GPI0 | CRT_DETECT | /GPI/ADC |
| GPI1 | PANEL_DETECT | /GPI/ADC |
| GPI2 | PLATFORM_ID | /GPI/ADC |
| GPI3 | CPPE# | /GPI/ADC |
| GPI4 | BAT_I | /GPI/ADC |
| GPI5 | BATT_TEMP | /GPI/ADC |
| GPI6 | ADAPTOR_1 | /GPI/ADC |
| GPI7 | BAT_V | /GPI/ADC |
| GPJ0 | EC_BL_ON | /GPI/DAC |
| GPJ1 | EC_PROCHOT | /GPI/DAC |
| GPJ2 | FAN_CTRL0 | /GPI/DAC |
| GPJ3 | CHG_REF | /GPI/DAC |
| GPJ4 | CHG_I | /GPI/DAC |
| GPJ5 | PWR_USB# | /GPI/DAC |

| Ivy Bridge CPU | | | | |
|----------------|-------------|--------|----|---------|
| | CPU CORE(V) | ICC(A) | W | TEMP(℃) |
| IMVP-7 | 1.05 | 33 | 17 | |
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| Panther Point | | | |
|---------------|----------|-------|---------|
| VCC | ICC(mA) | W | TEMP(℃) |
| +3.3V | 262 | 0.87 | 105 |
| +1.8VS | 3249 | 5.73 | |
| +1.5V | 86 | 0.129 | |
| +1.05 | 14688.52 | 15.43 | |

| Panther Point | | | |
|---------------|---------|--------|---------|
| VCC | ICC(mA) | mW | TEMP(℃) |
| +5V | 4 | 20 | 70 |
| +5VS | 2 | 10 | |
| +3.3V | 347 | 1145.1 | |
| +3.3VS | 212 | 699.6 | |
| +1.5V | 1988 | 2982 | |
| +1.05V | 1634 | 1715.7 | |

| ITE8518 | | | |
|---------|---------|-----|---------|
| VCC | ICC(mA) | mW | TEMP(℃) |
| +3.3V | 100 | 330 | 70 |

| IDT92HD87B | | | |
|-------------|---------|------|---------|
| VCC | ICC(mA) | mW | TEMP(℃) |
| +3.3V(DVDD) | 200 | 660 | 70 |
| +5V(AVDD) | 1000 | 5000 | |

| ADM1032 | | | |
|---------|-------|------|---------|
| VCC | ICC | mW | TEMP(℃) |
| +3.3V | 170uA | 0.56 | 150 |

| JMC251 | | | |
|--------|---------|-----|---------|
| VCC | ICC(mA) | mW | TEMP(℃) |
| +3.3VS | 300 | 990 | 70 |
| +1.2VS | 150 | 180 | |
| | | | |

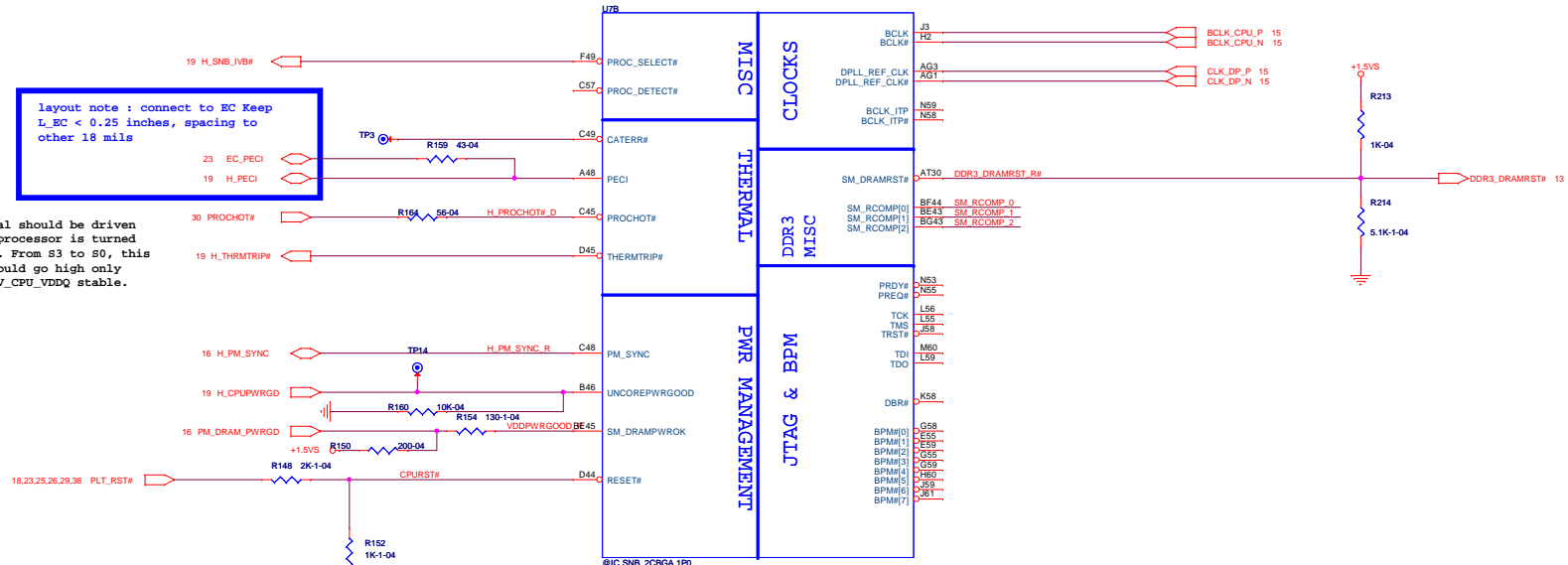
SANDYBRIDGE PROCESSOR(DMI,PEG,FDI)



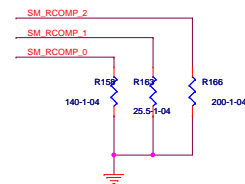
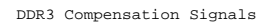
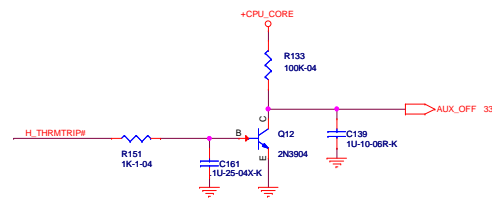
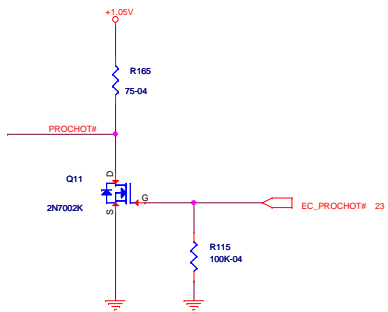
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)

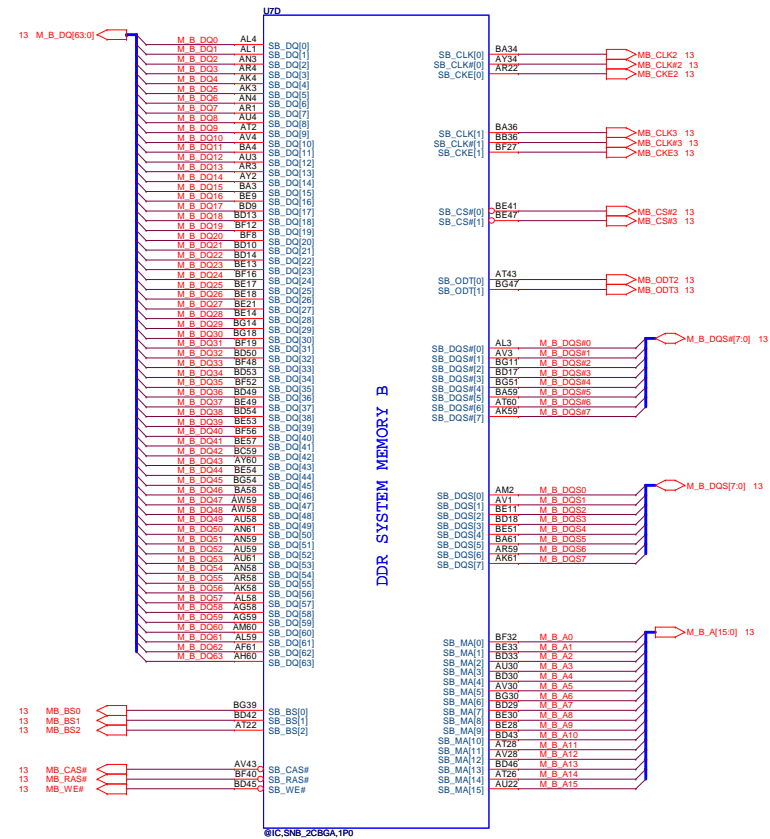
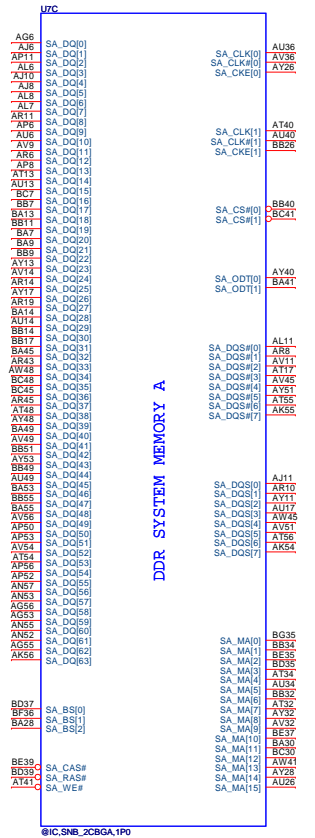
This pin is for compability with future platforms. A pull up resistor to VCPLL is required if connected to the DF_TV5 strap on the PCH.



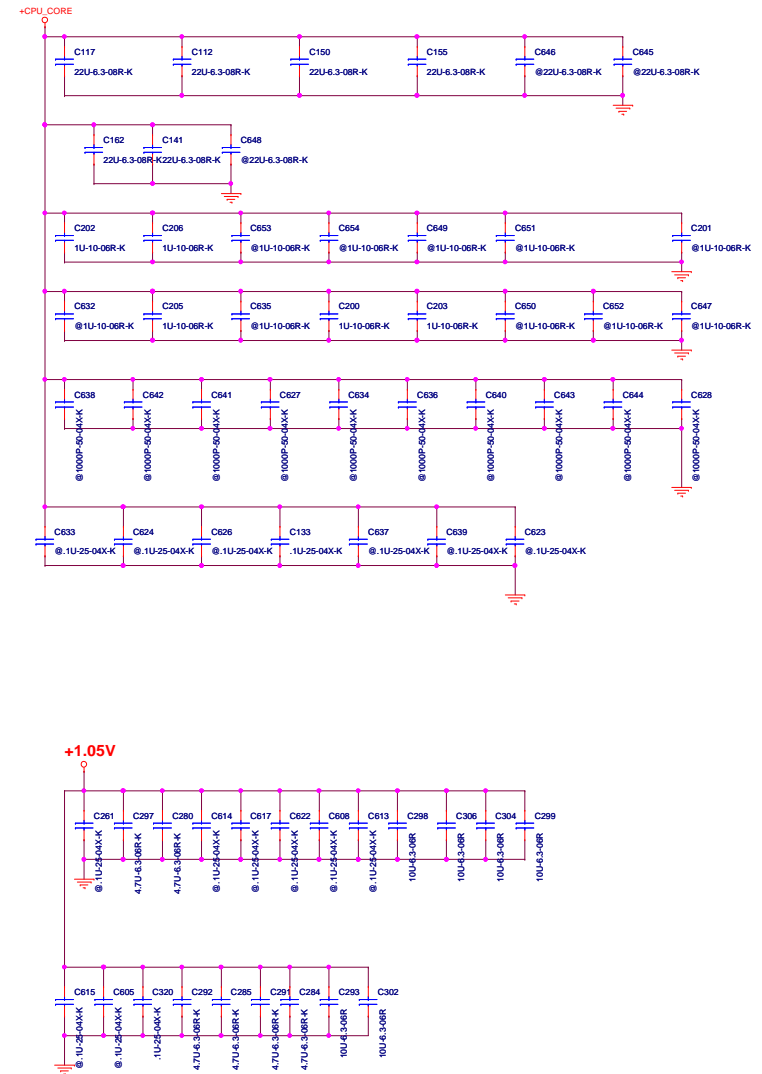
This signal should be driven low when processor is turned off in S3. From S3 to S0, this signal should go high only after 1.5V_CPU_VDDQ stable.



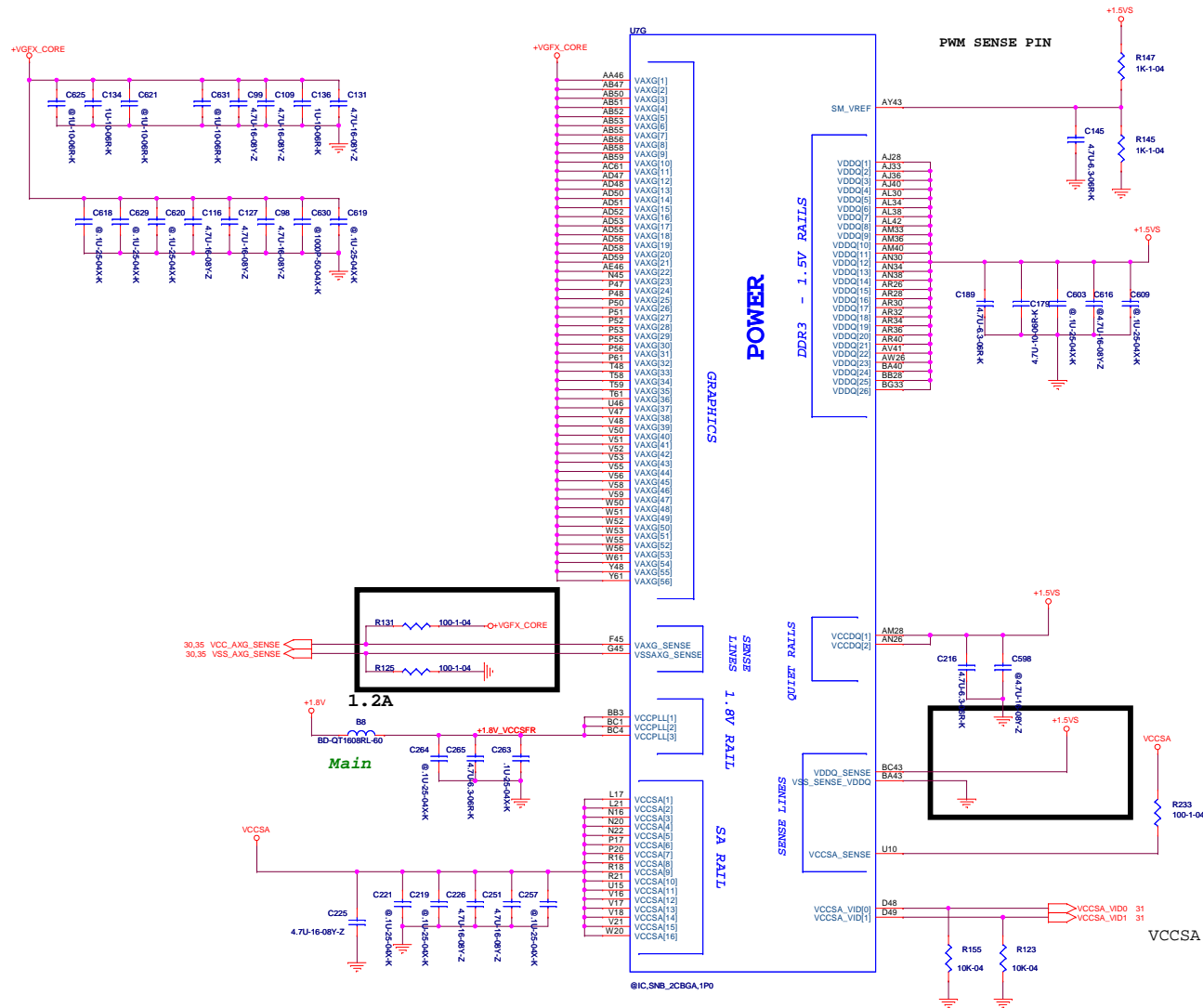
SANDYBRIDGE PROCESSOR (DDR3)



+CPU_Core Decoupling



IVY BRIDGE PROCESSOR (POWER)



0.85V PWM SENSE PIN

IVY BRIDGE PROCESSOR (VSS)

UTM

VSS

UTM

VSS

NCTF

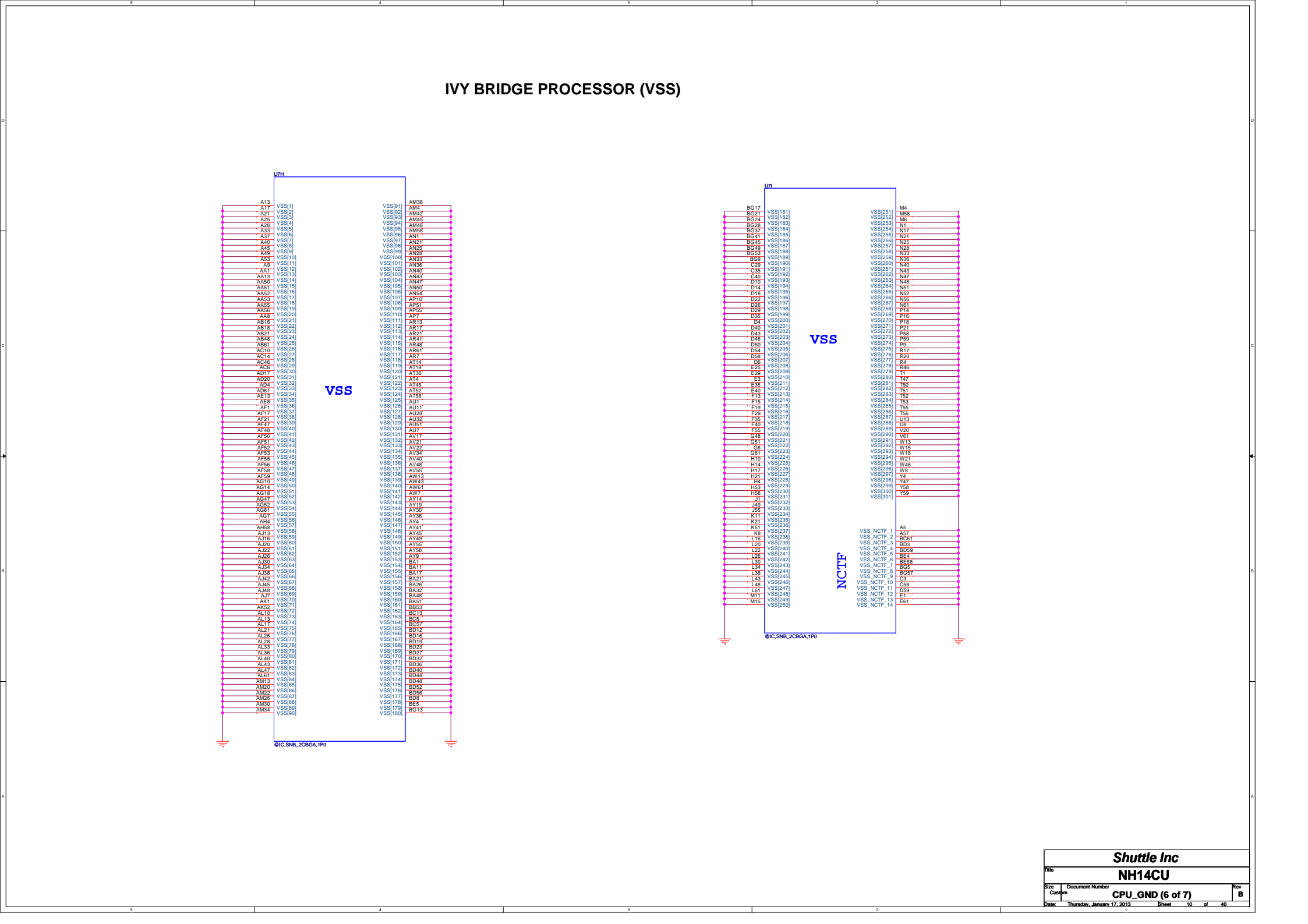
SHUTTLE INC

NH14CU

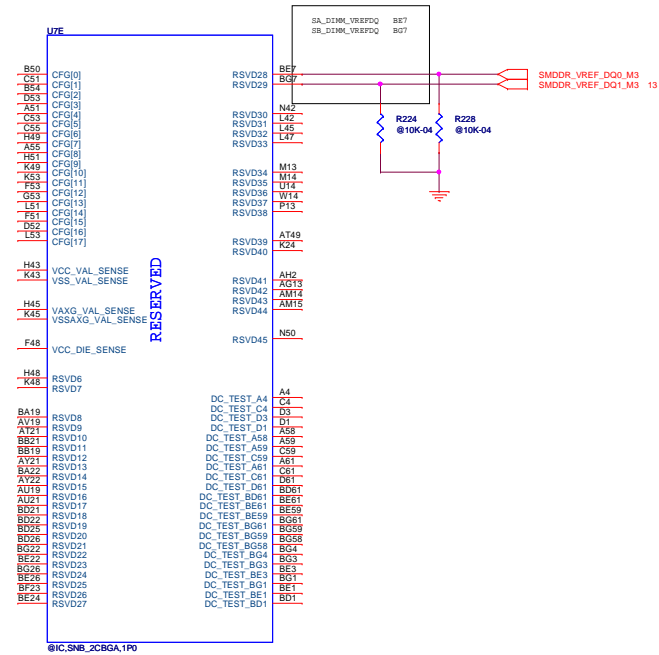
CPU_GND (6 of 7)

Thursday, January 17, 2013

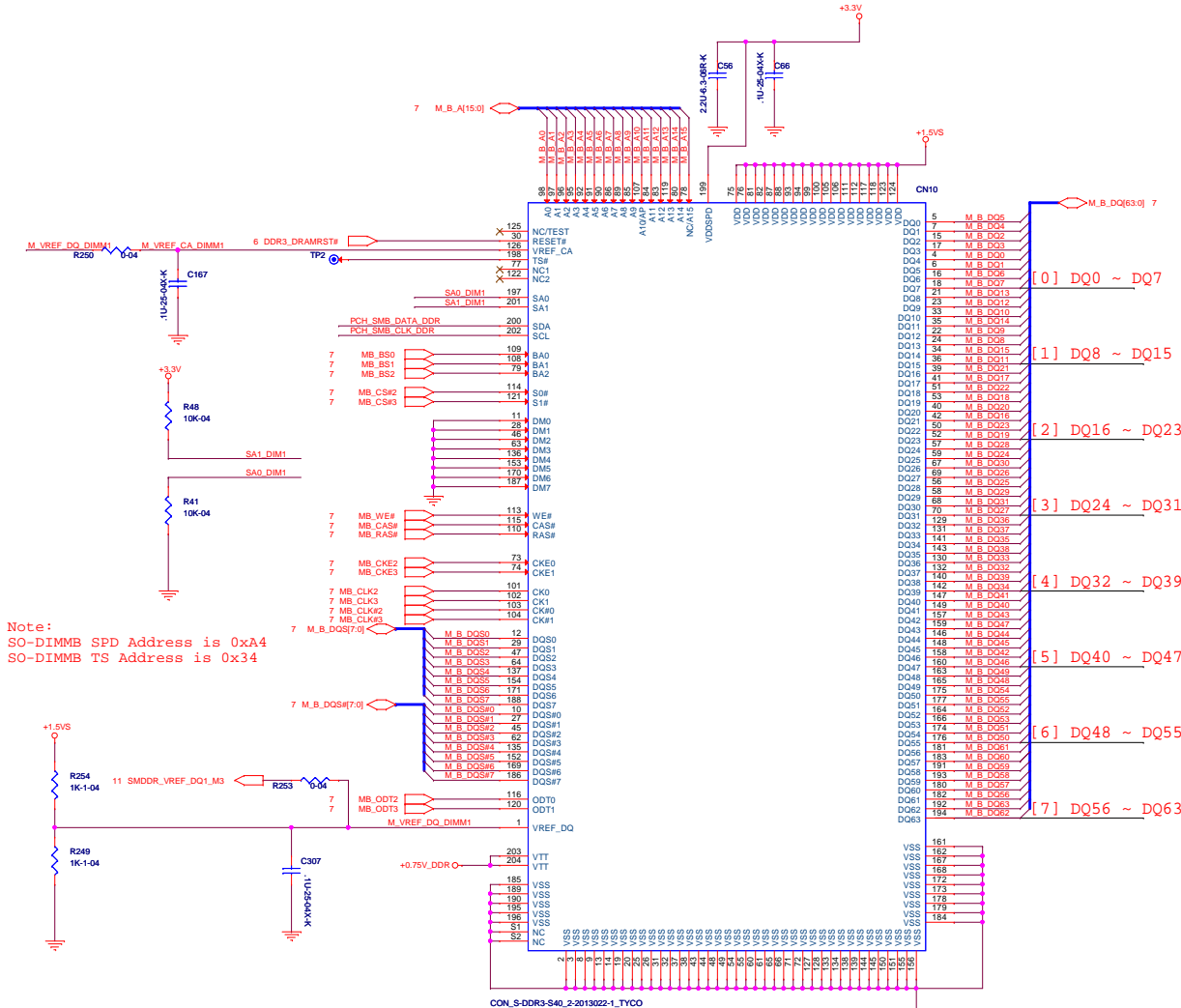
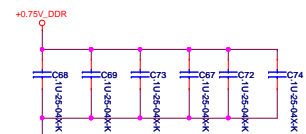
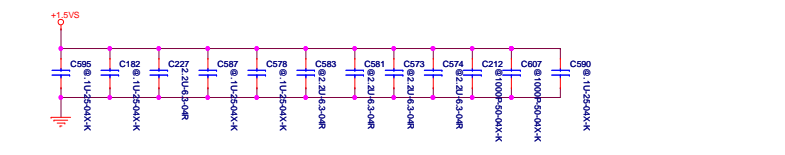
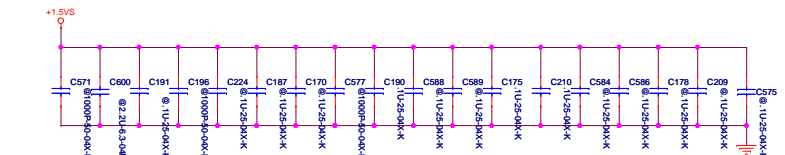
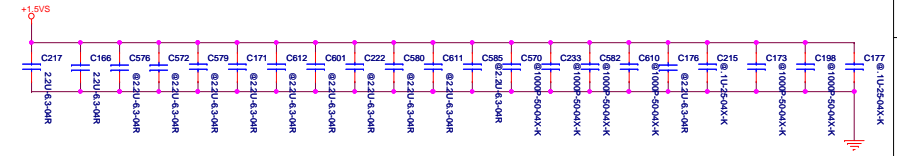
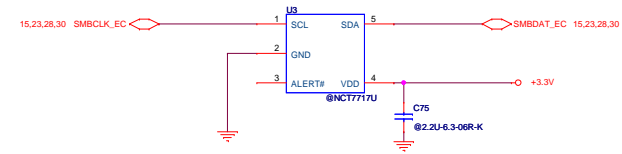
Sheet 10 of 40



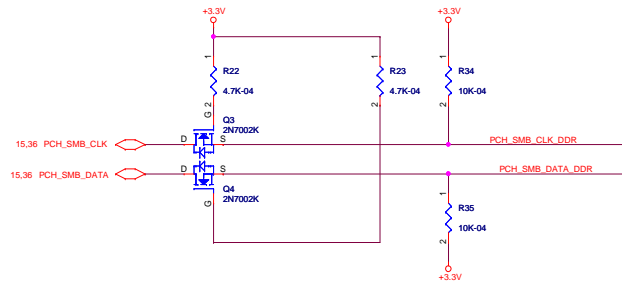
| | | | |
|----------------------------------|---|-----------------|--|
| Shuttle Inc | | | |
| Title NH14CU | | | |
| Size Custom | Document Number CPU_RESERVED (7 of 7) | Rev B | |
| Date: Thursday, January 17, 2013 | Sheet 11 of 40 | | |



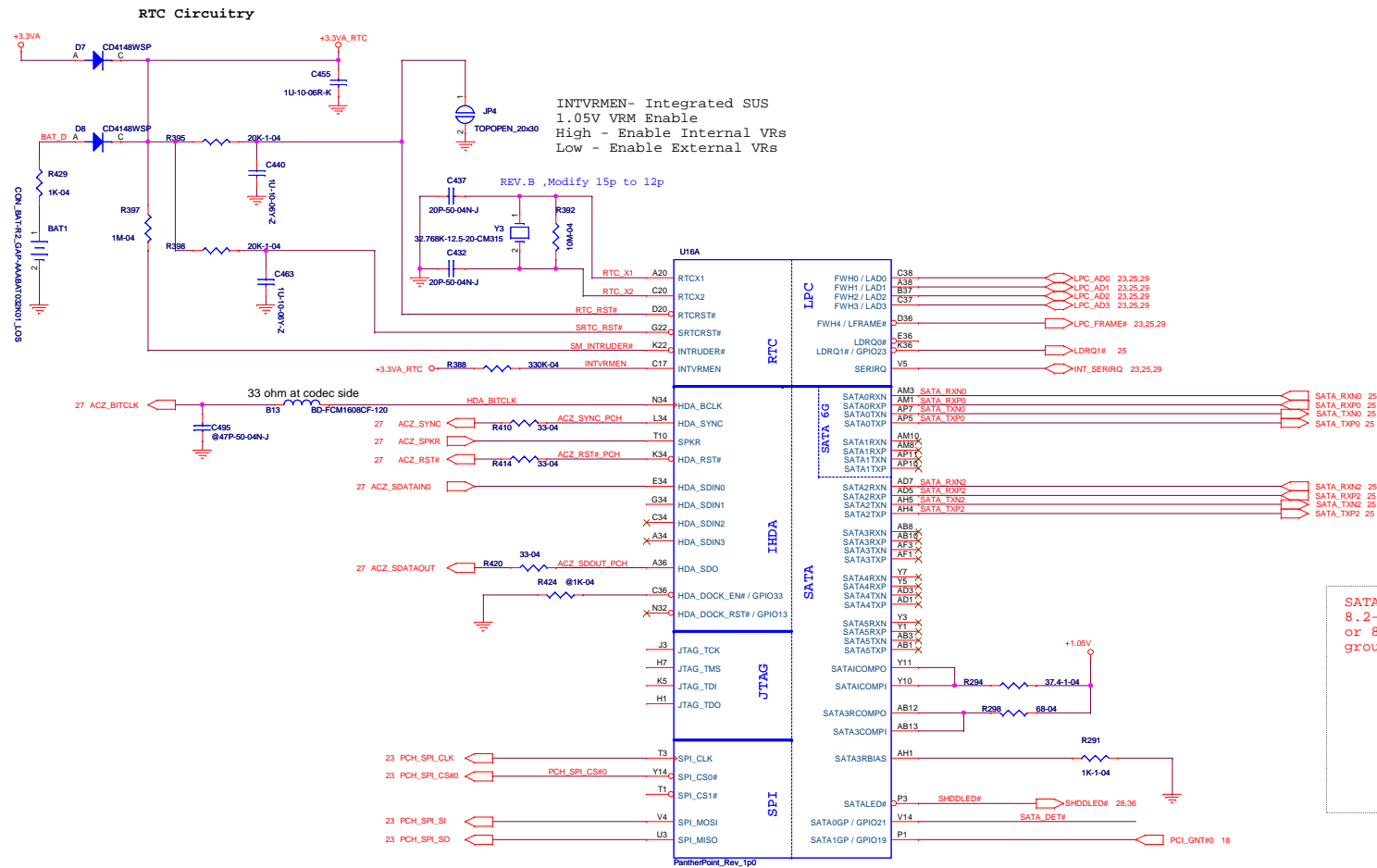
CPU Thermal Sensor



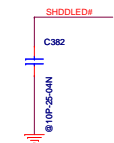
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34



Panther Point Chipset (RTC,LPC,SATA,HDA,SPI,JTAG)

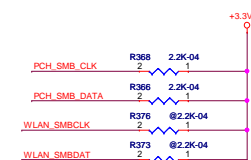
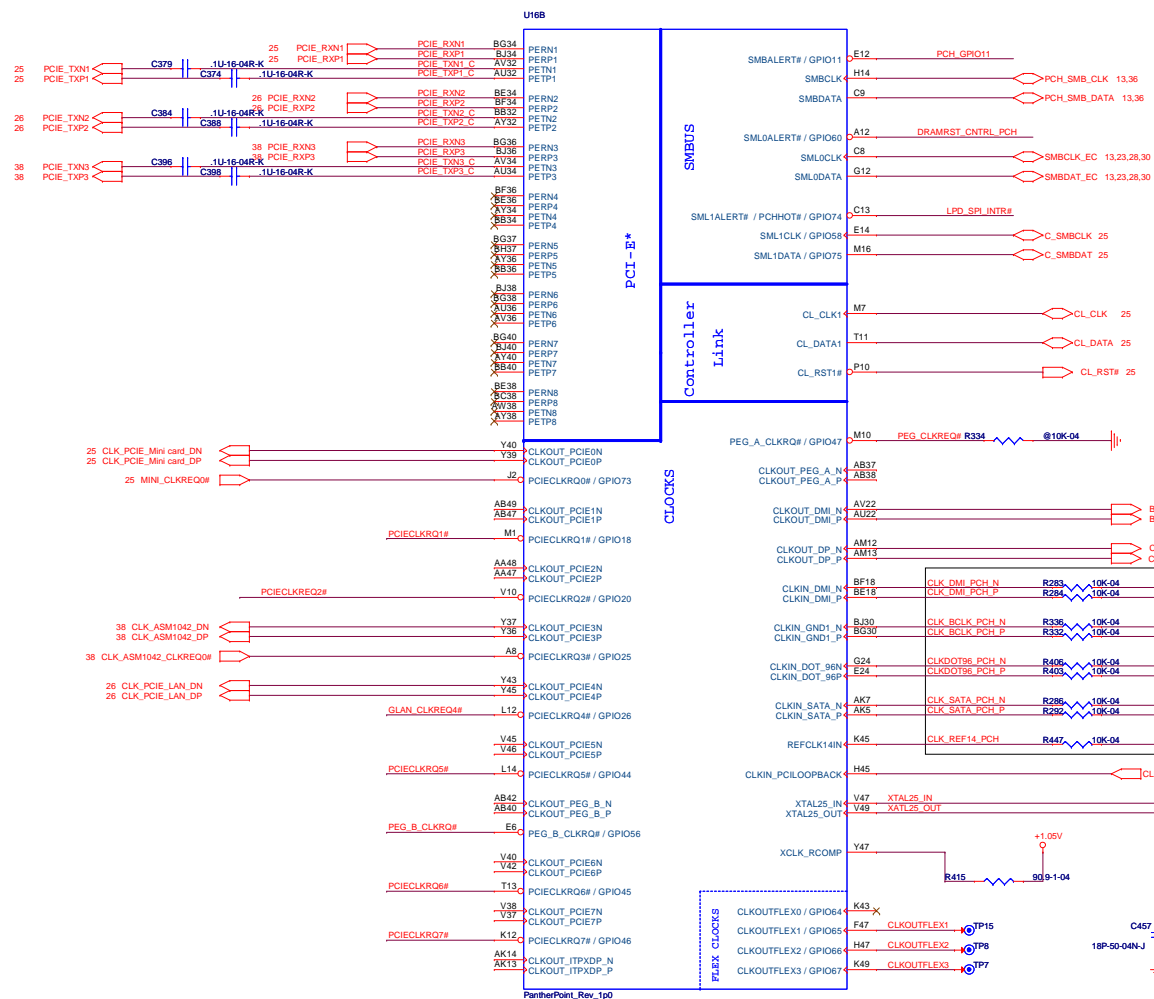


SATA[x]GP pins if unused require 8.2-k to 10-k pull-up to +Vcc3_3 or 8.2-k to 10-k pull-down to ground.



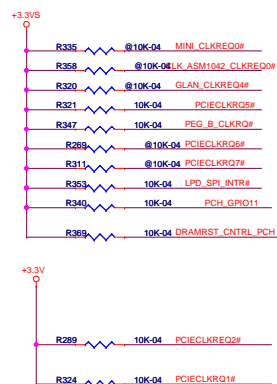
Panther Point Chipset (PCIE,SMBUS,CLOCK)

| USB | Location |
|--------|----------------|
| PCIE 1 | WLAN |
| PCIE 2 | LAN+cardreader |
| PCIE 3 | USB3.0 |
| PCIE 4 | no use |
| PCIE 5 | no use |
| PCIE 6 | no use |
| PCIE 7 | no use |
| PCIE 8 | no use |

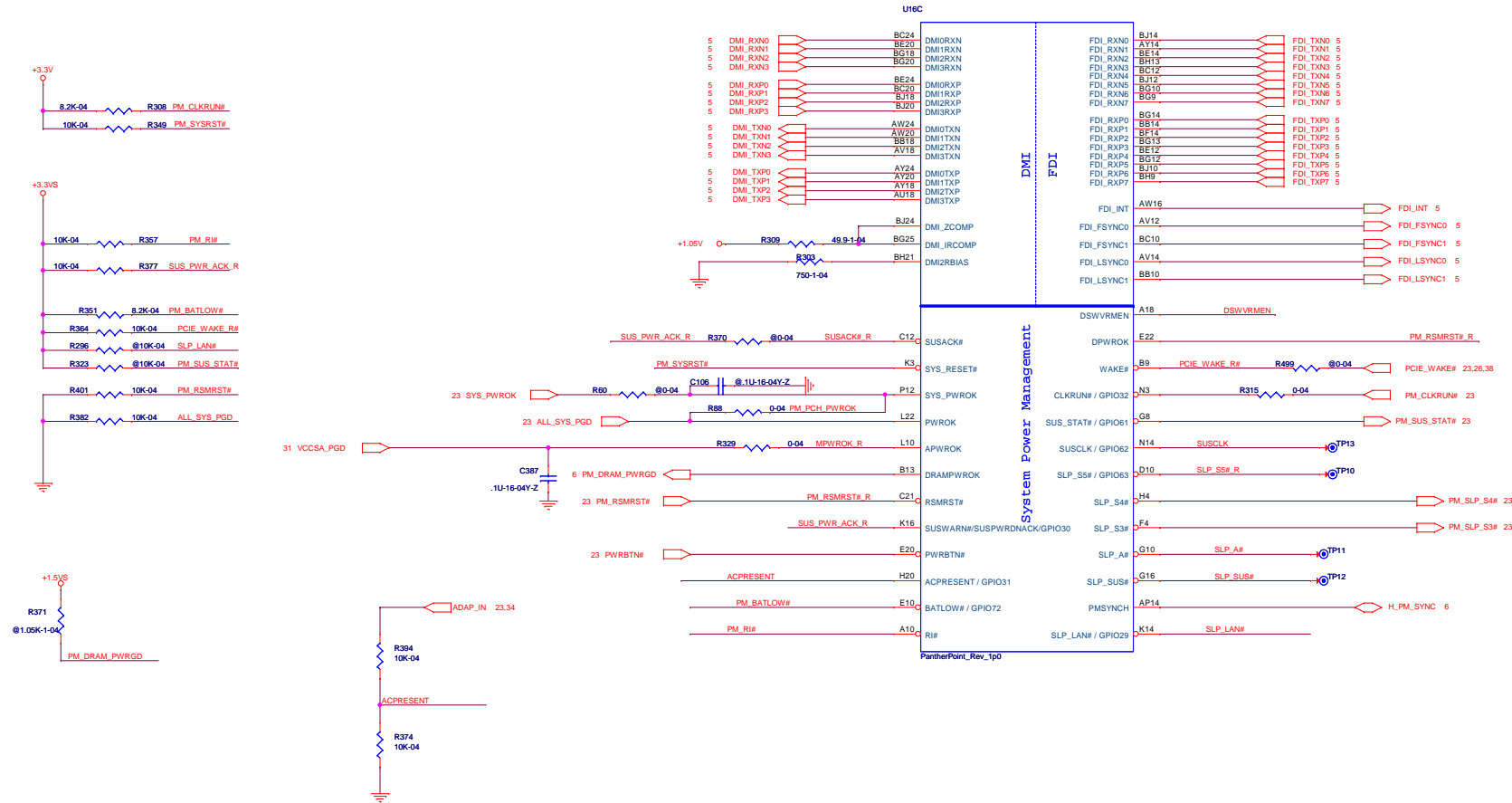


| | |
|--------------|----------|
| SMB_ | DDRA,DDR |
| SML0_ | n/a |
| SML1_ | to EC |

This input has to be terminated with a 10-kOhms pull-down termination resistor in Integrated Clock generation mode.



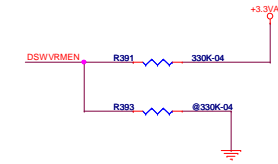
Panther Point Chipset (DMI,FDI)

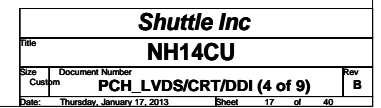


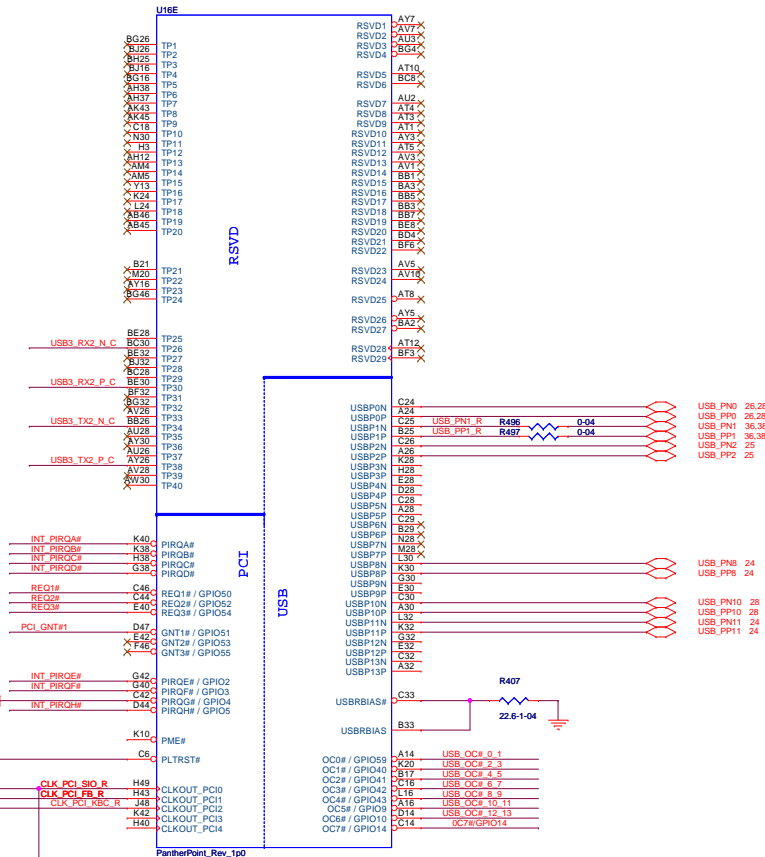
DSWODVREN - On Die DSW VR Enable

HIGH Enabled (DEFAULT) Enabled (DEFAULT)
(R132 STUFFED, R128 UNSTUFFED)

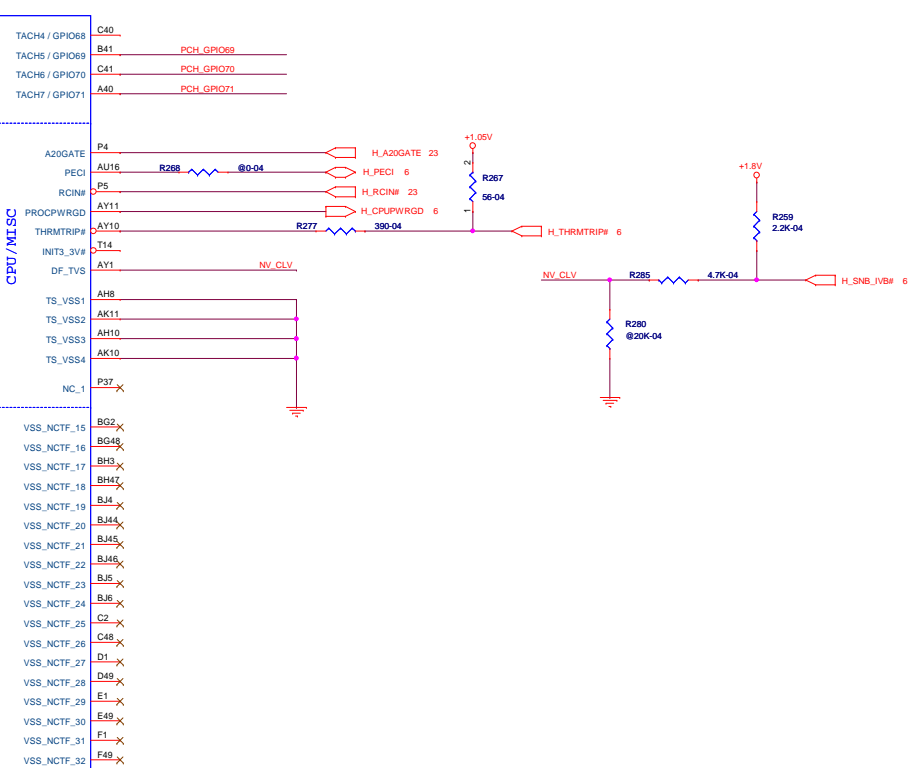
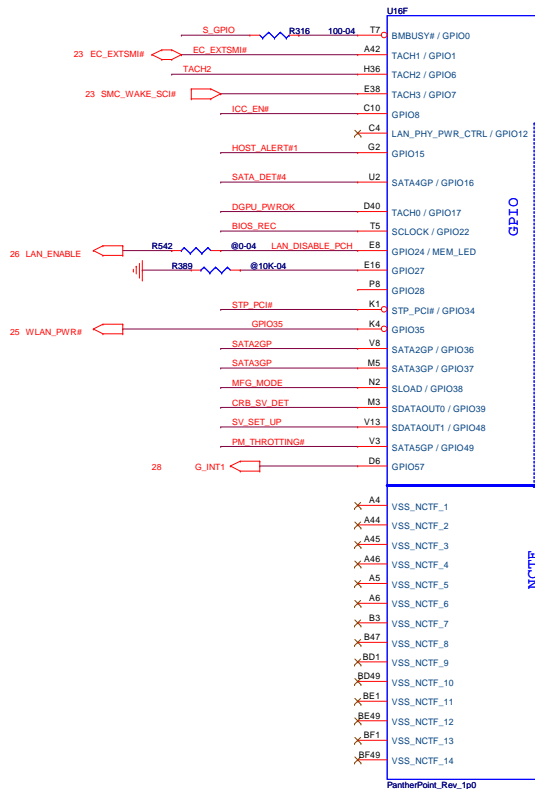
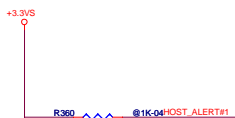
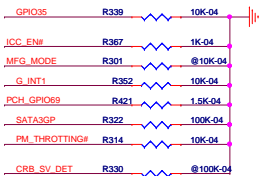
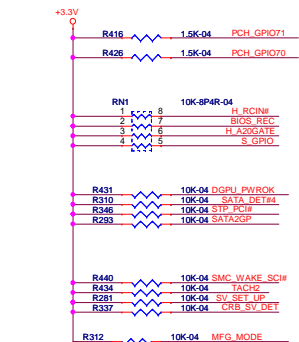
LOW Disabled (R128 STUFFED, R132 UNSTUFFED) Disabled

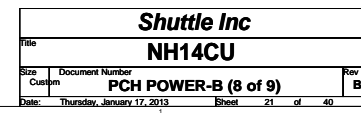


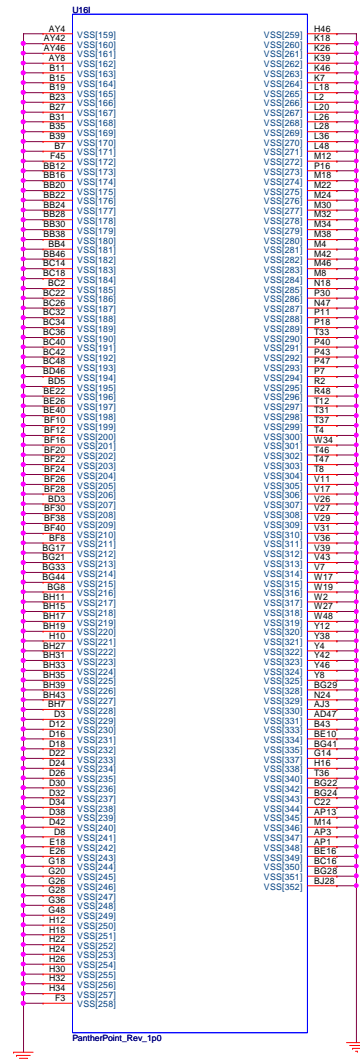
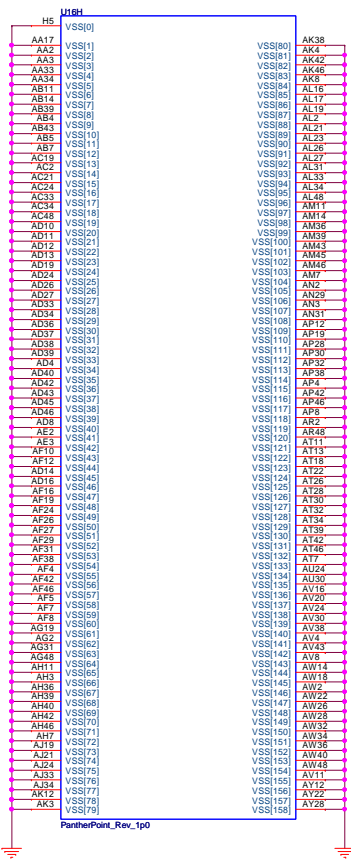


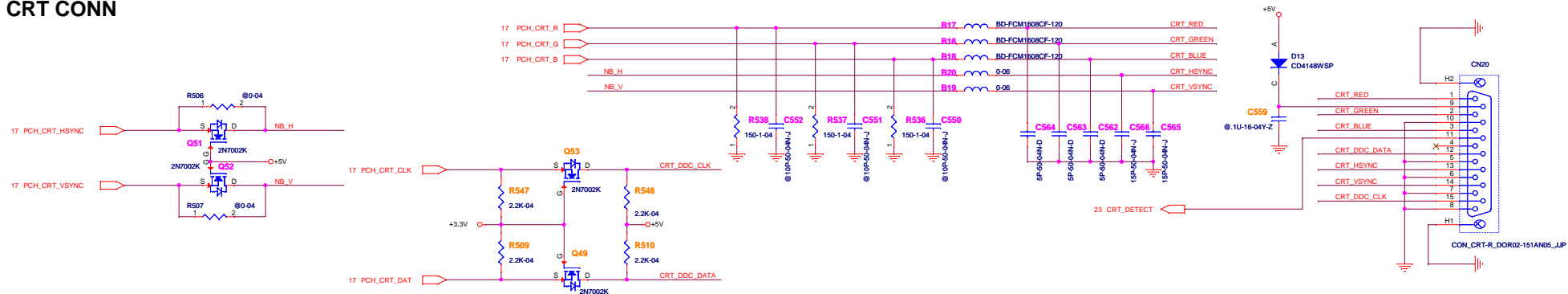


The schematic diagram illustrates the USB to RS-485 interface circuit. It features a USB to UART bridge IC (MAX3232CPE) connected to a USB port (USB_OC# 0..11, USB_OC# 6..7, OC7#/GPIOD14). The IC is also connected to an RS-485 transceiver IC (RS485CPE). The RS-485 transceiver is connected to an RS-485 network (R396, R381) and a +3.3V supply. The RS-485 network is connected to a microcontroller (MCU) via a 10K-O4 resistor.



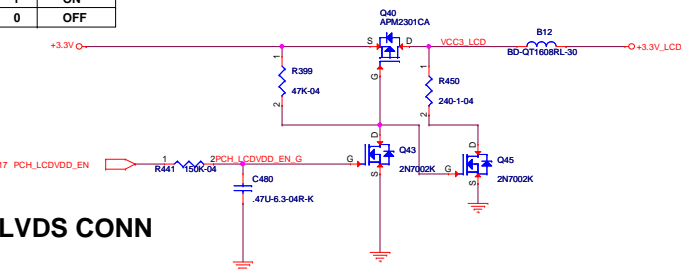




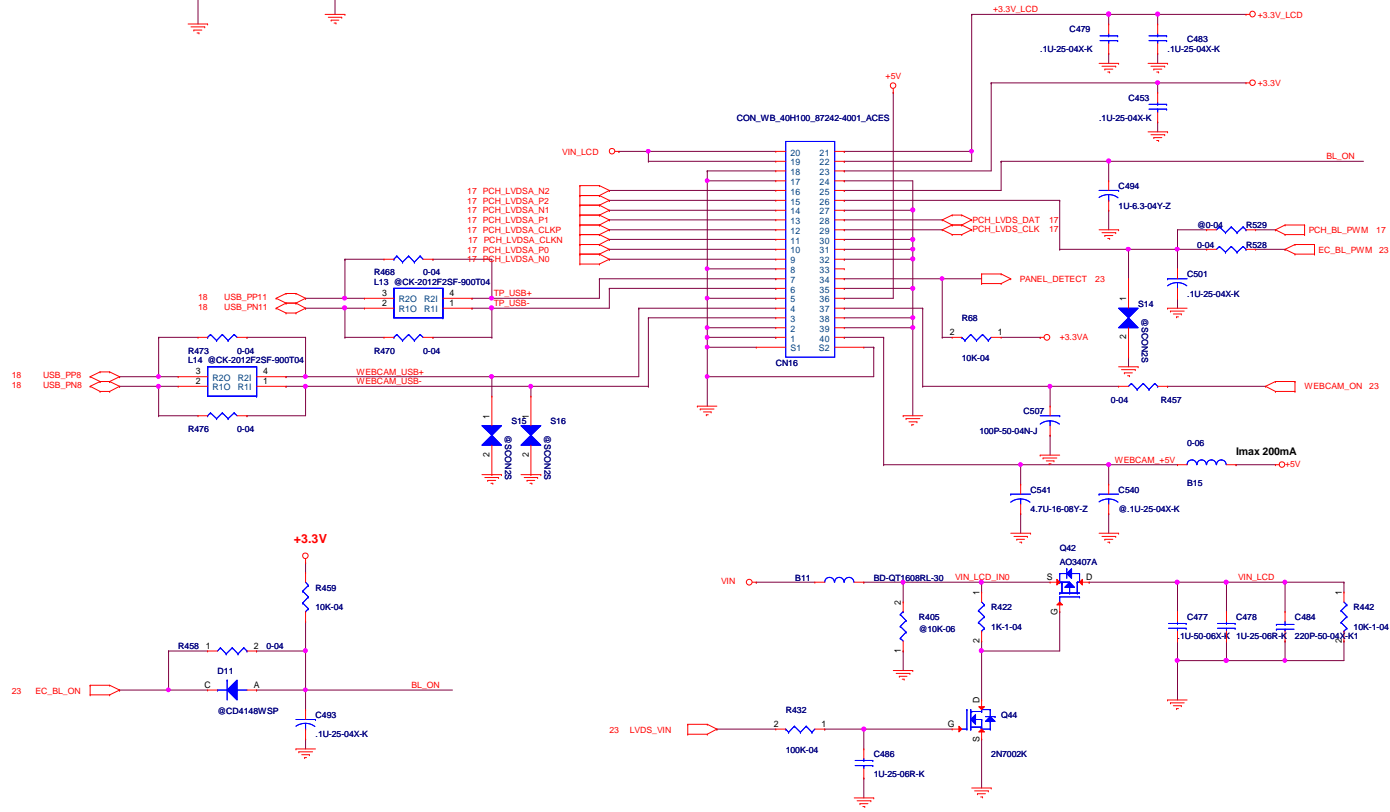
CRT CONN

Webcam CONN

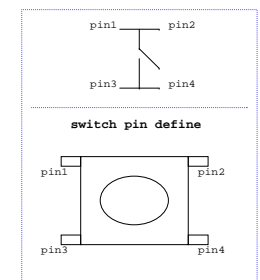
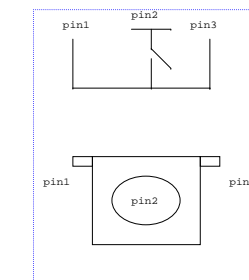
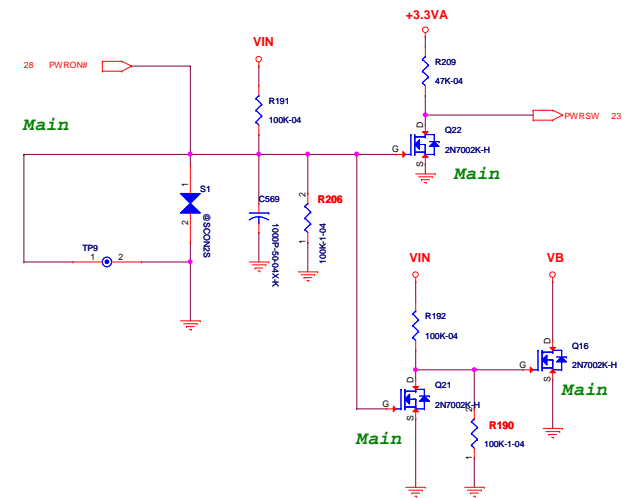
| WEBCAM_ON | |
|-----------|-----|
| 1 | ON |
| 0 | OFF |



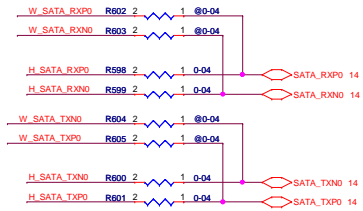
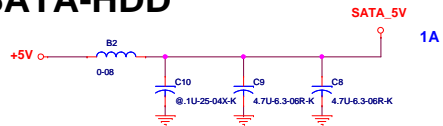
Co-Lay with LVDS 30 PIN Conn
50pin conn symbol no stuff



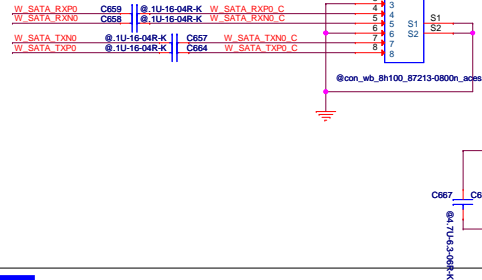
PWR SW



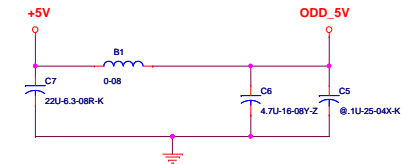
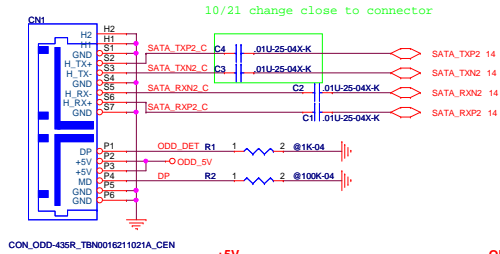
SATA-HDD



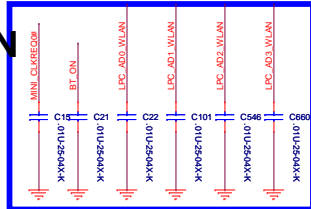
HDD Cable



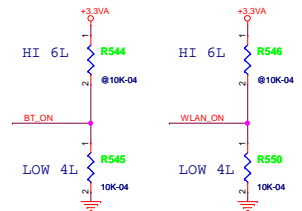
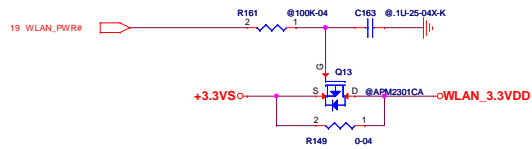
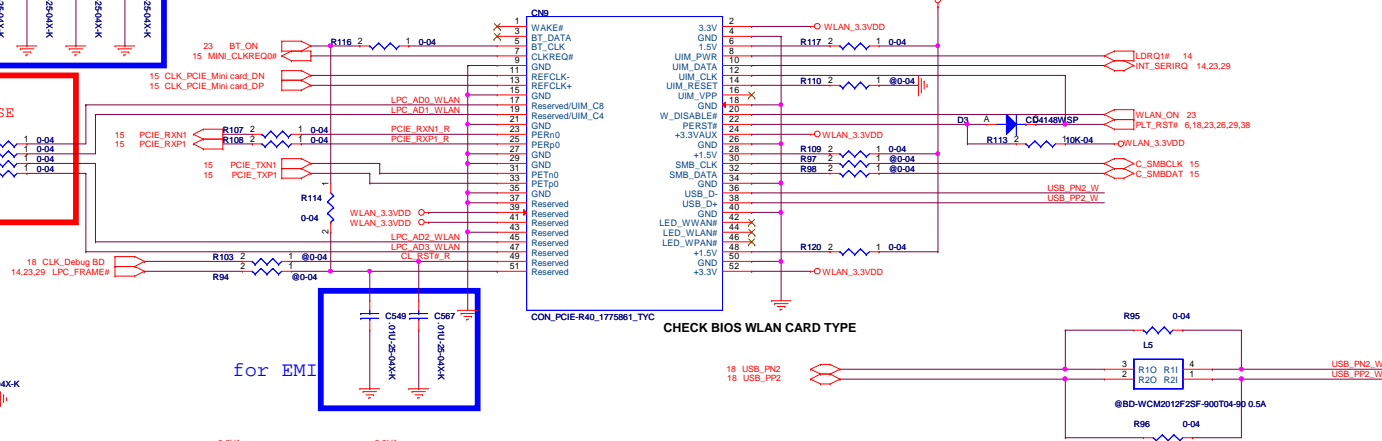
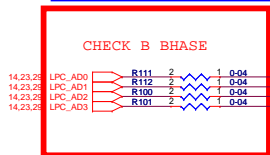
CD-ROM



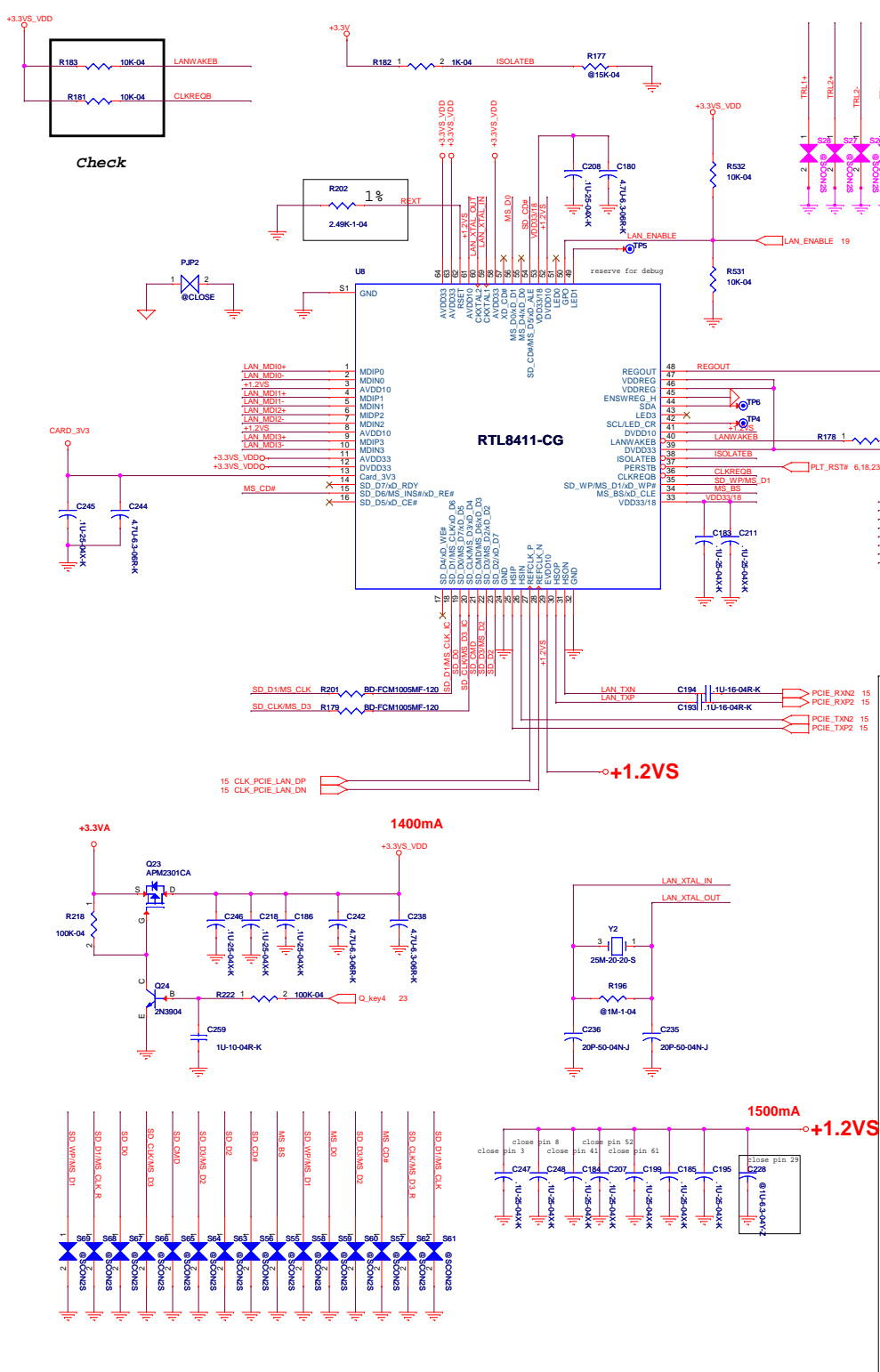
MINI CARD CONN



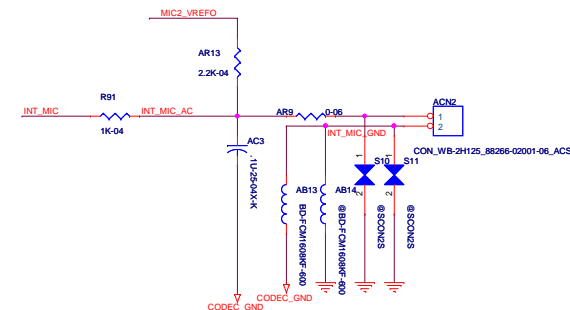
for EMI



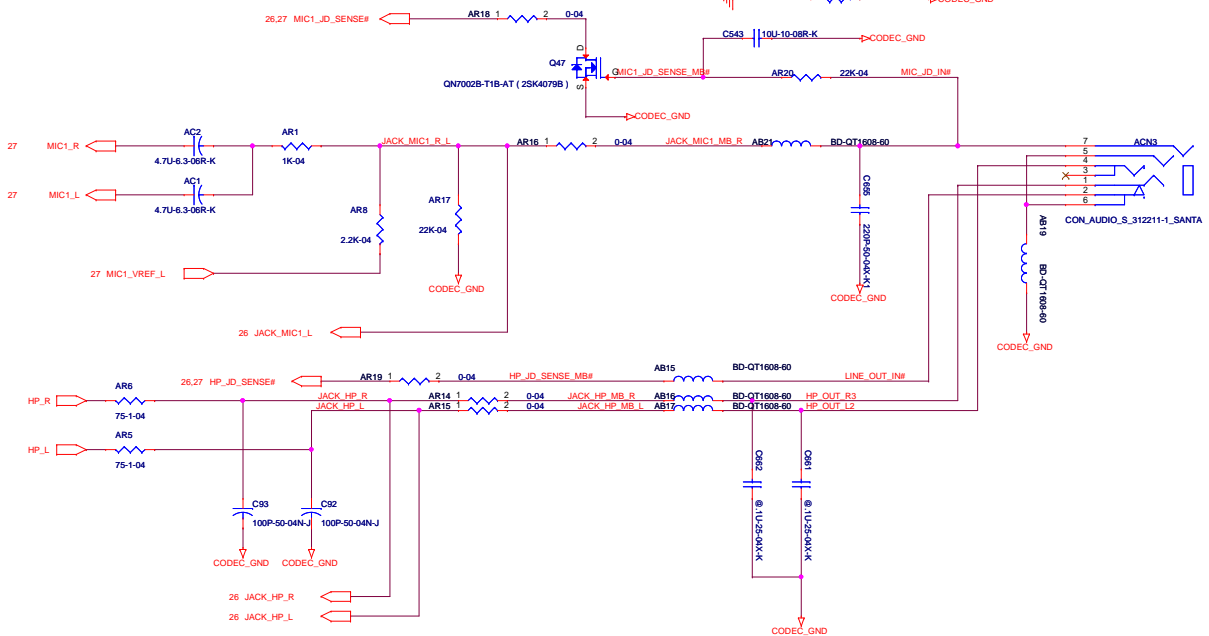
```
BT_ON (LED) HI= LED DB
                LOW= On Board LED
WLAN_ON(FAN) HI= 6L
                LOW= 4L
```



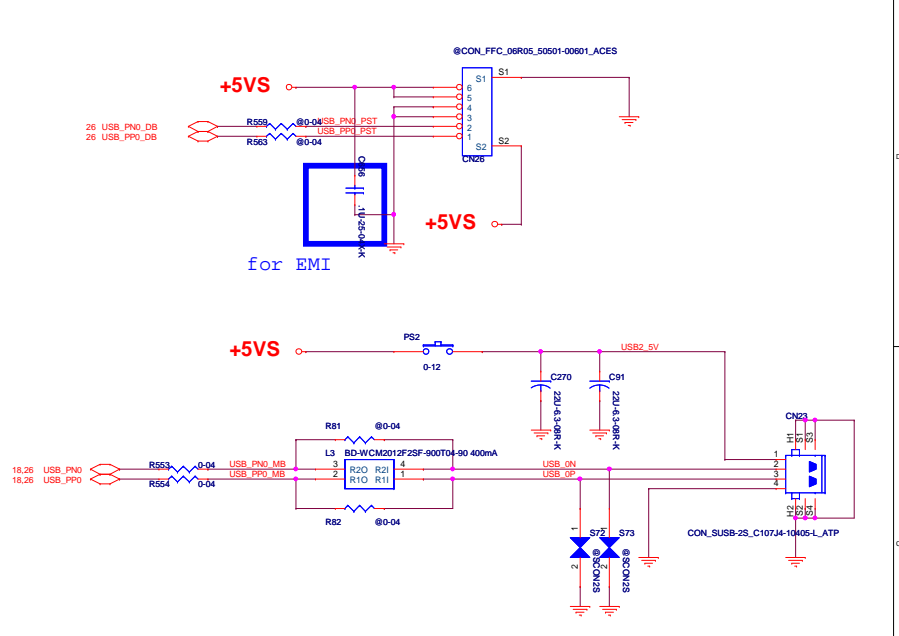
AMP VDD



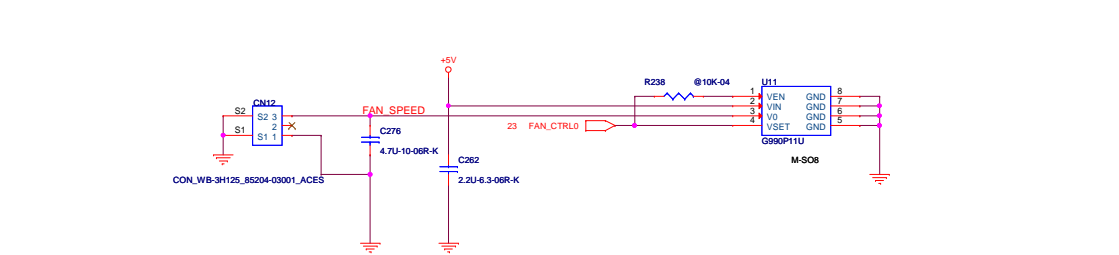
2 IN 1 Audio Jack / USB



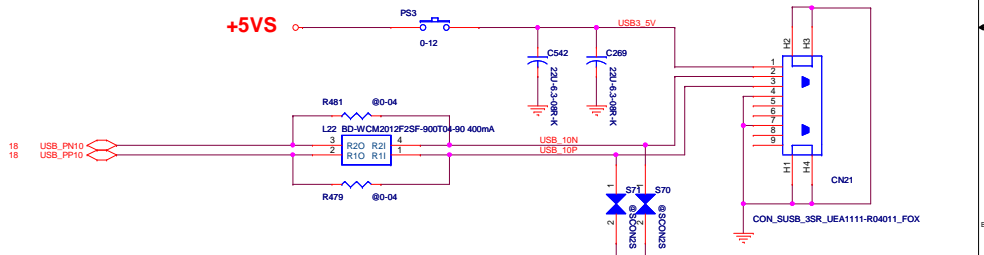
USB2.0(Include 15" DB)



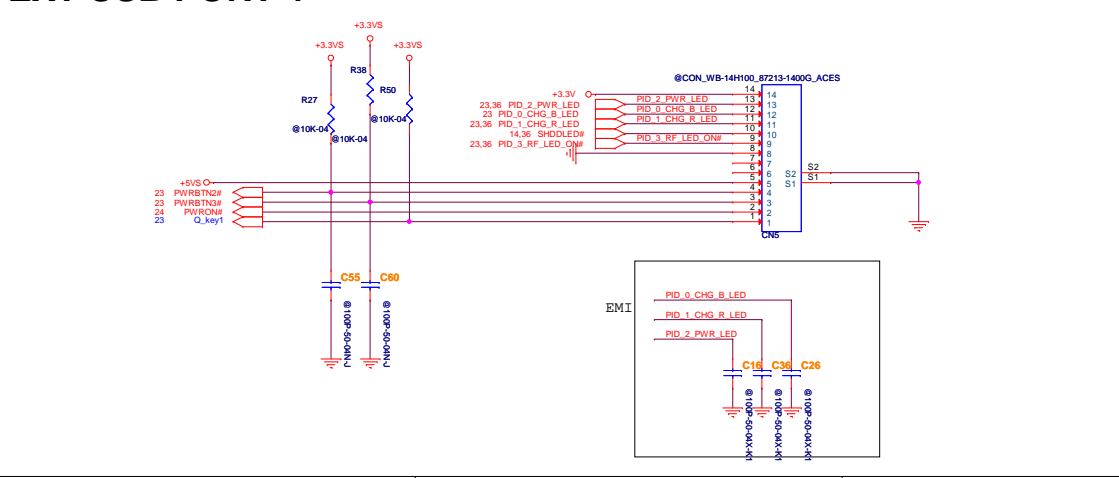
FAN CONTROLLER



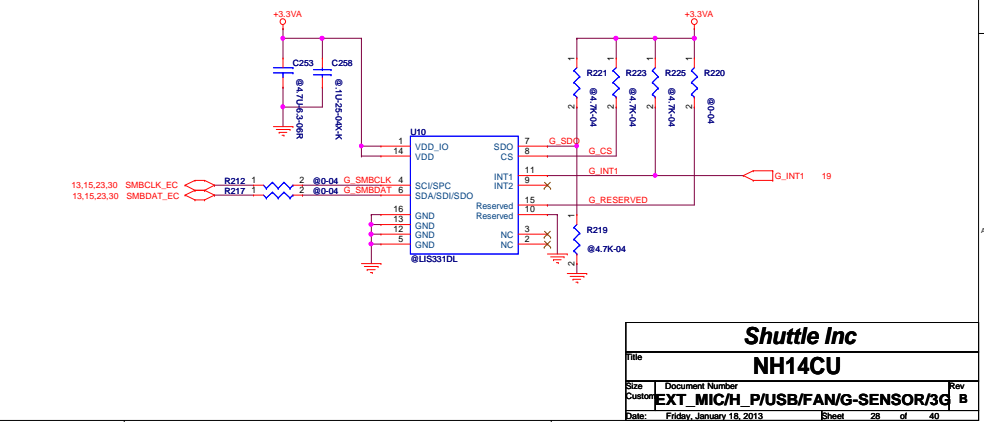
USB2.0

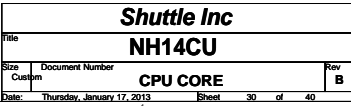


EXT USB PORT 4

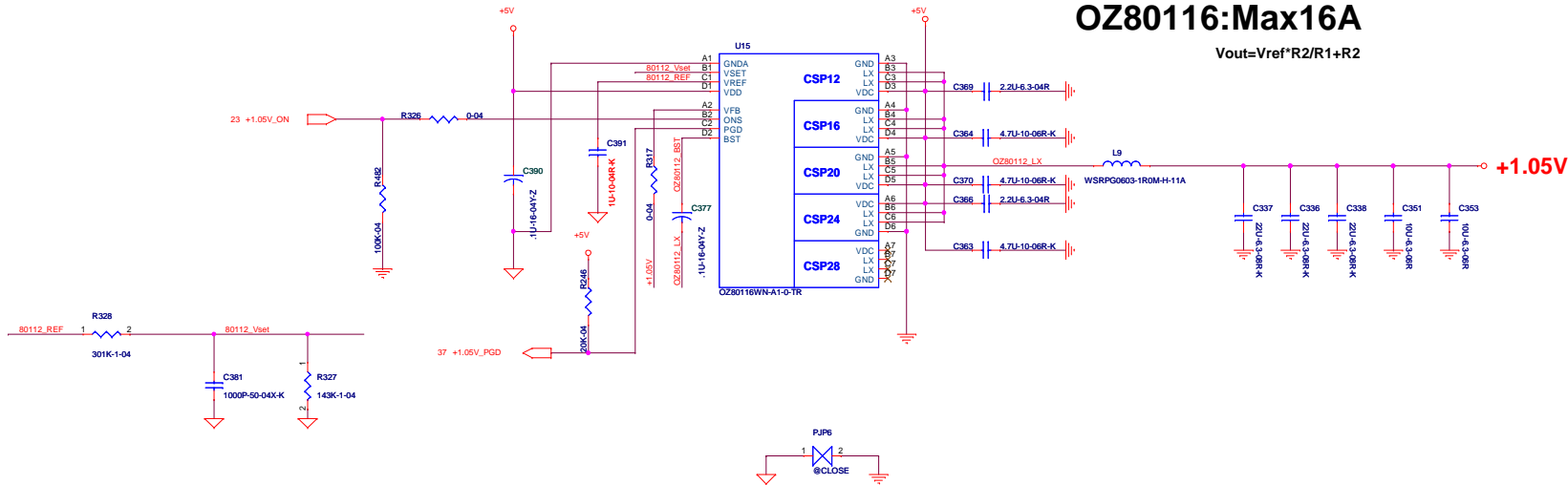


G SENSOR

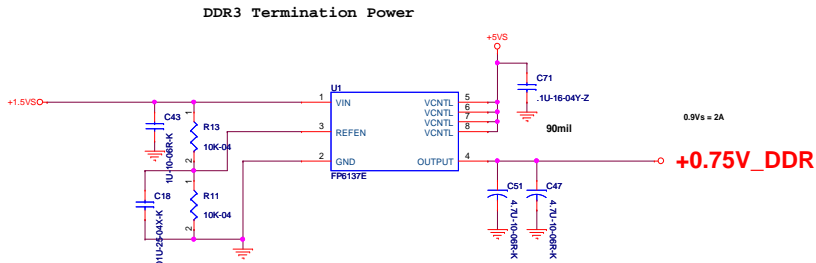




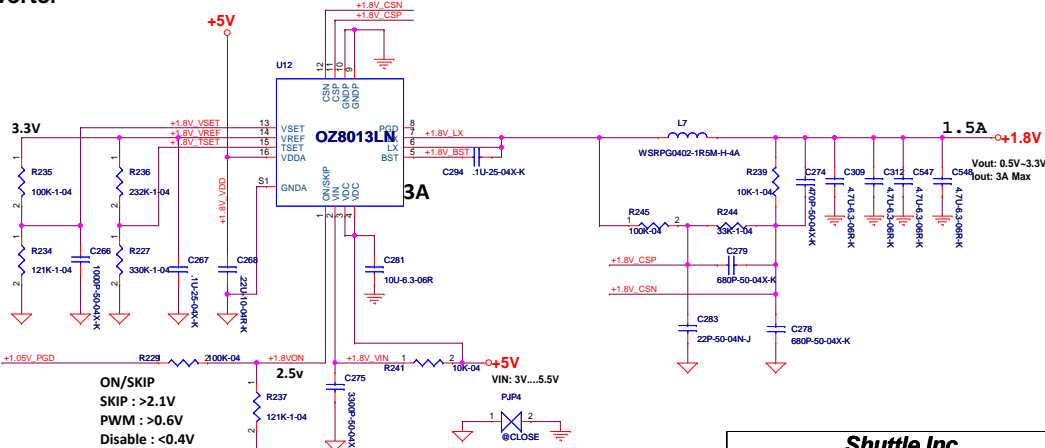
1.05V PWM



0.75VS LDO

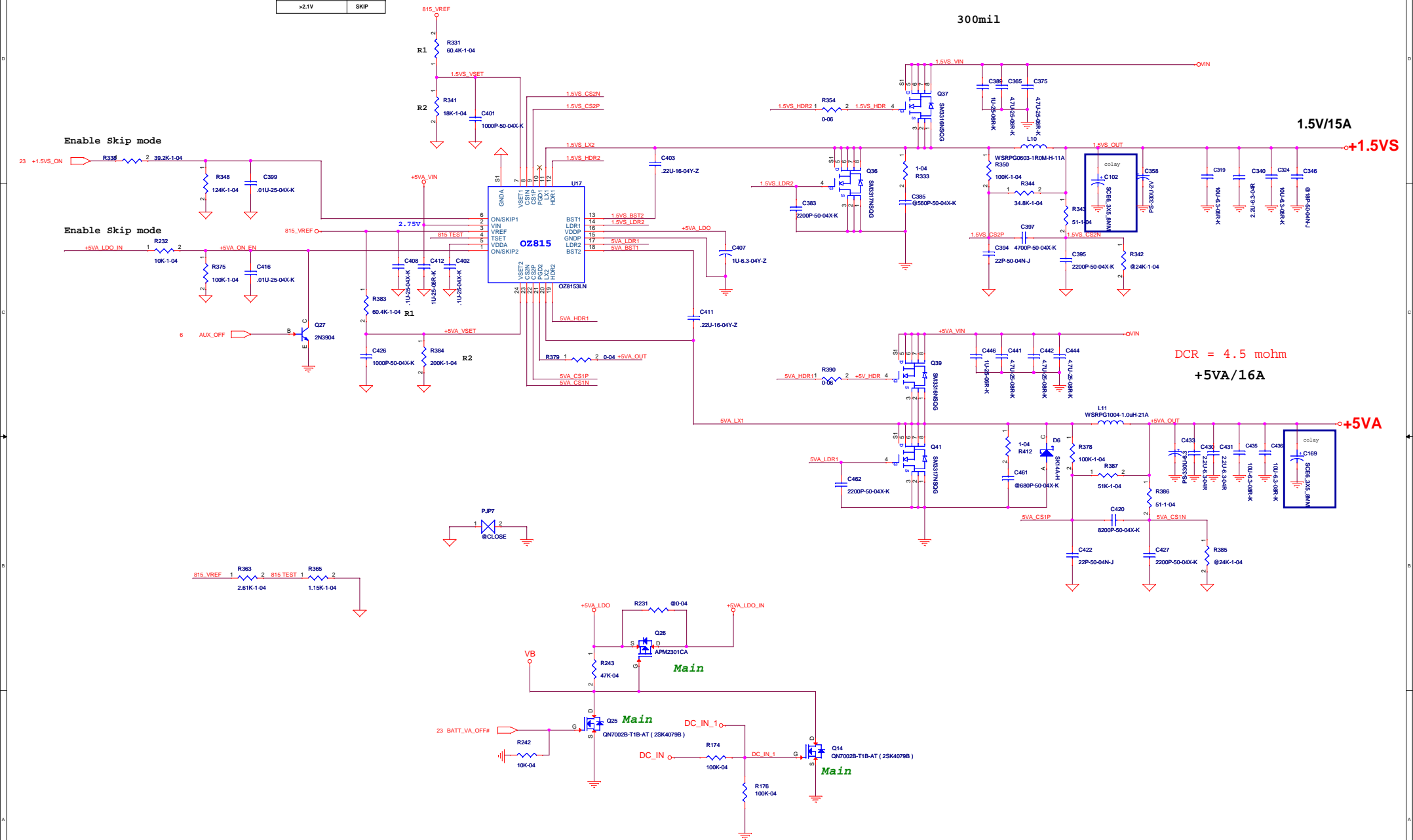


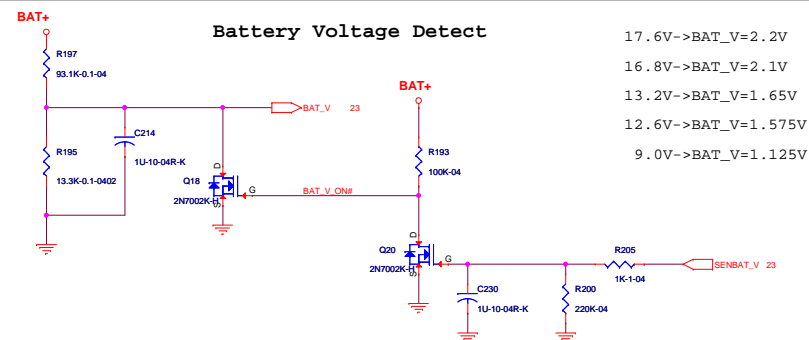
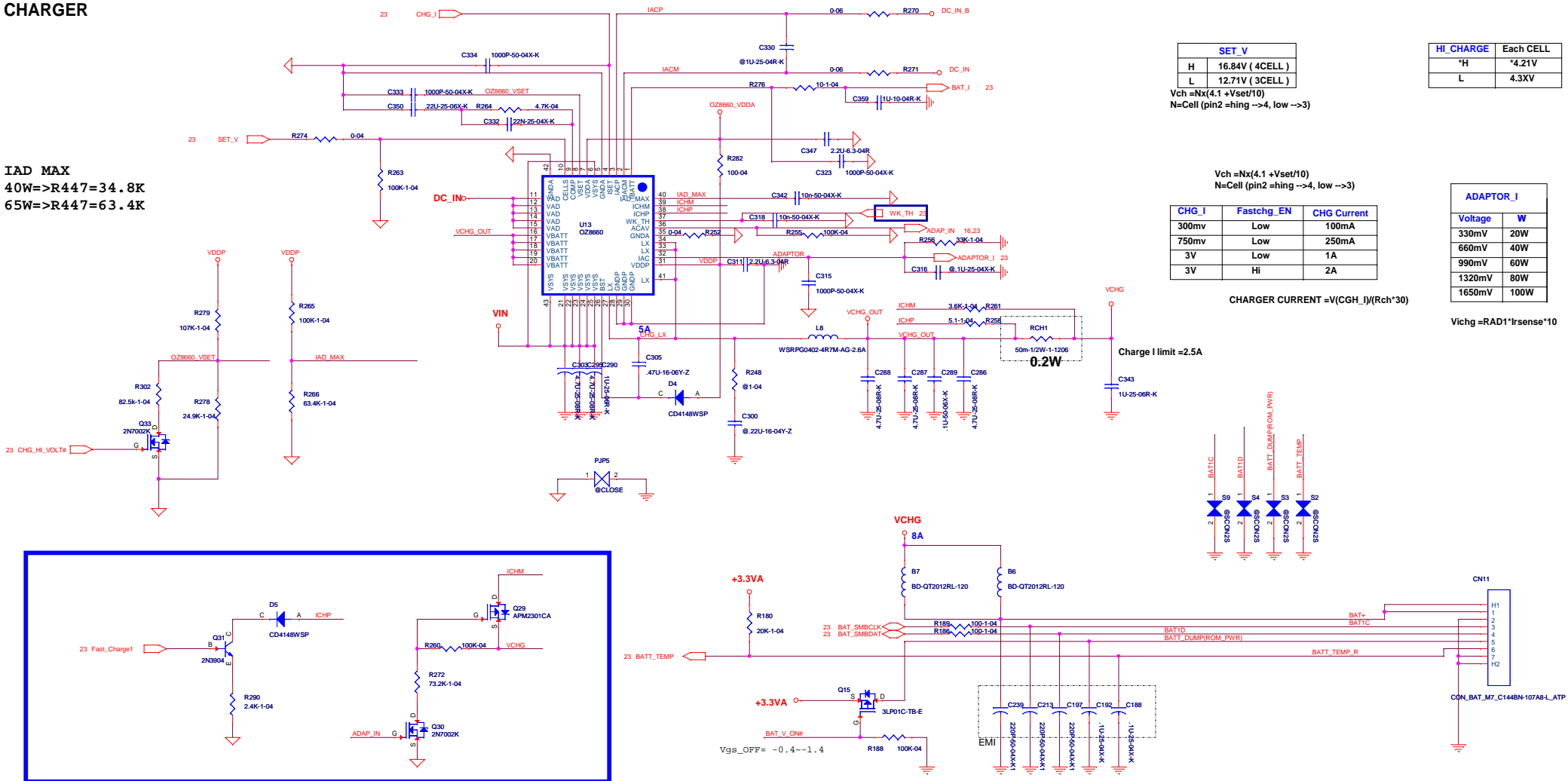
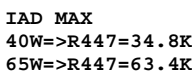
1.8V Converter



| +1.8V/+5V_ON Voltage | Mode |
|----------------------|------|
| <0.4V | OFF |
| >0.6V | PWM |
| >2.1V | SKIP |

Output Voltage = [Vref x R2/(R1+R2)] x 2

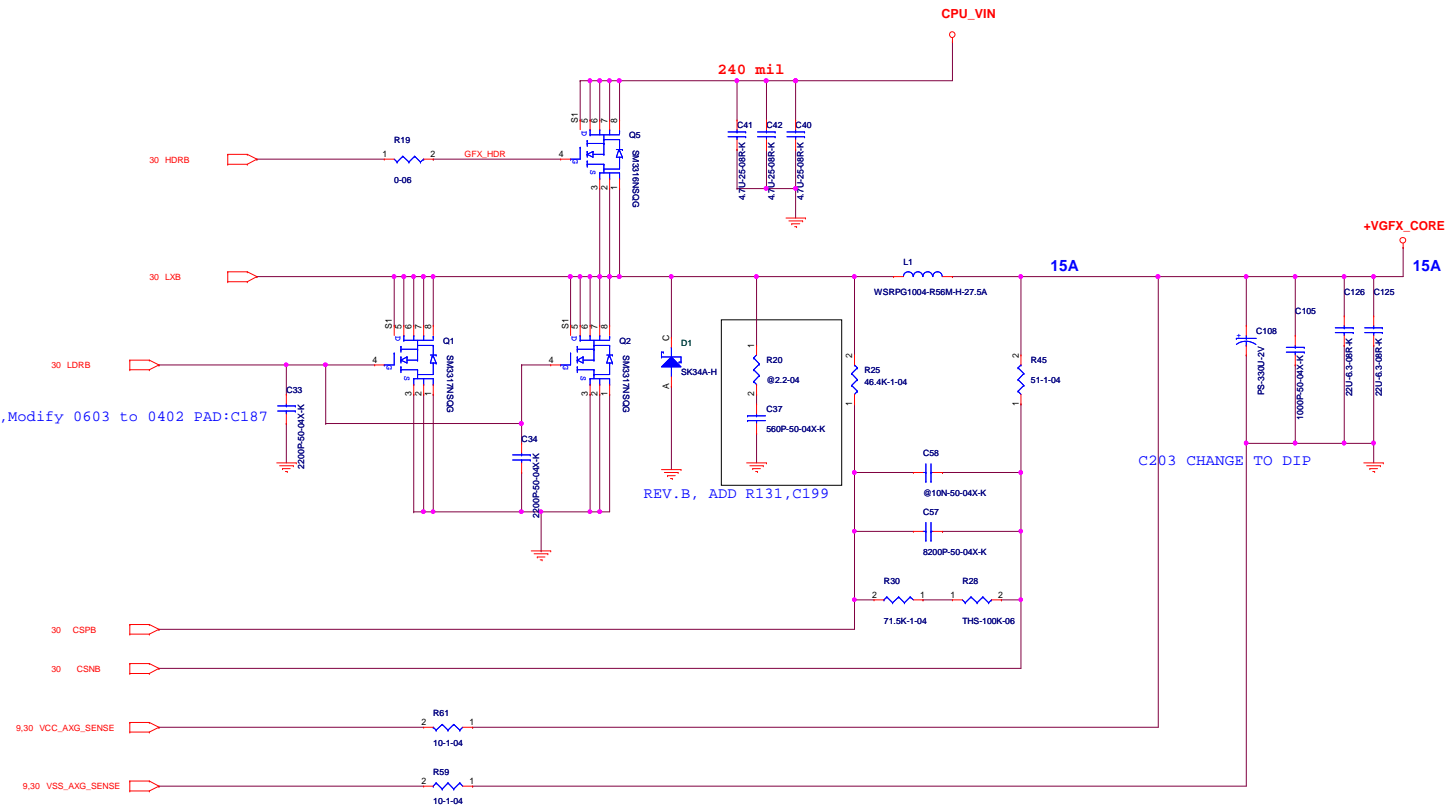


CHARGER

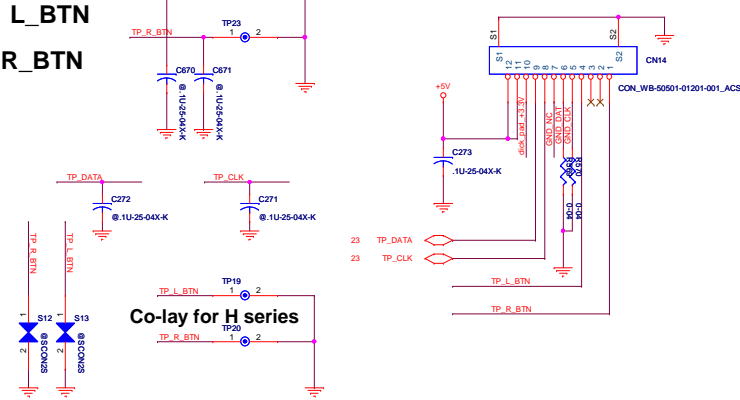
REV.B,Modify 0603 to 0402 PAD:C187

REV.B, ADD R131,C199

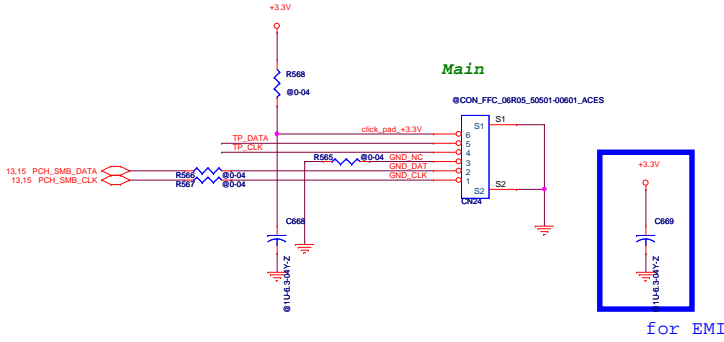
C203 CHANGE TO DIP



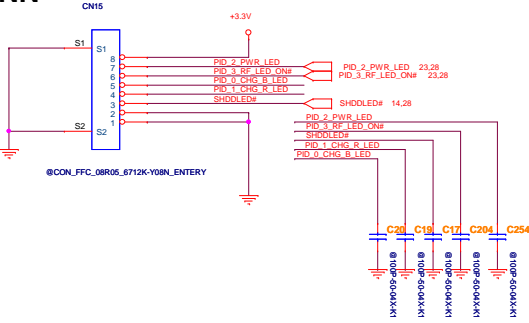
Touch Pad



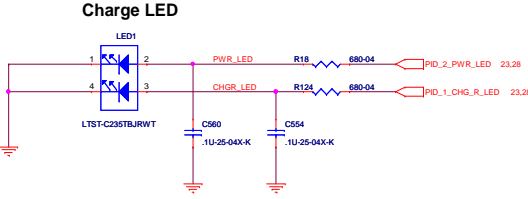
Click-pad / Co-LAY with Touch-pad



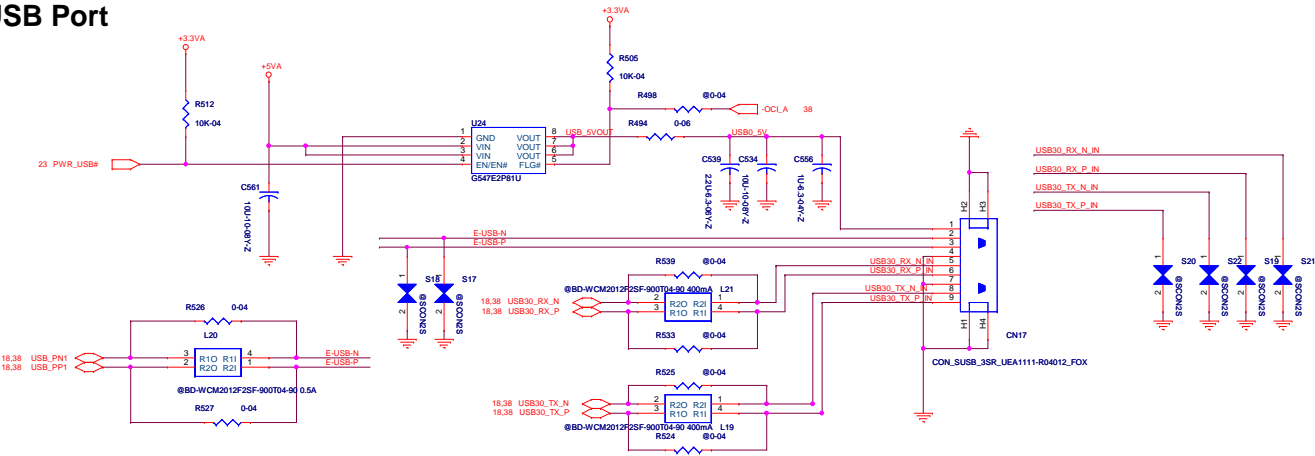
LED CONN



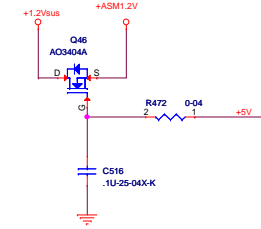
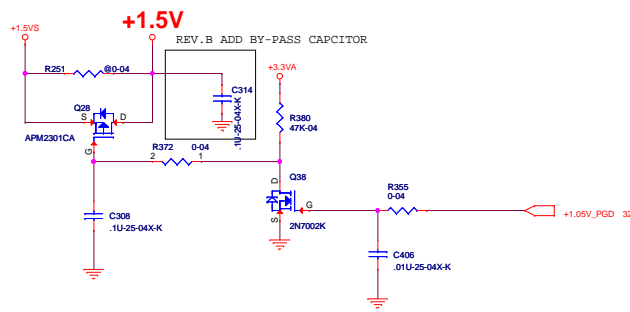
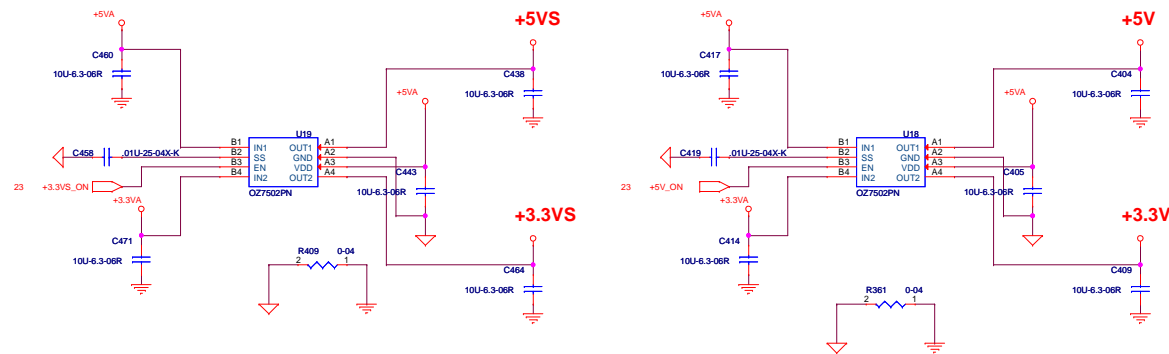
H-LED



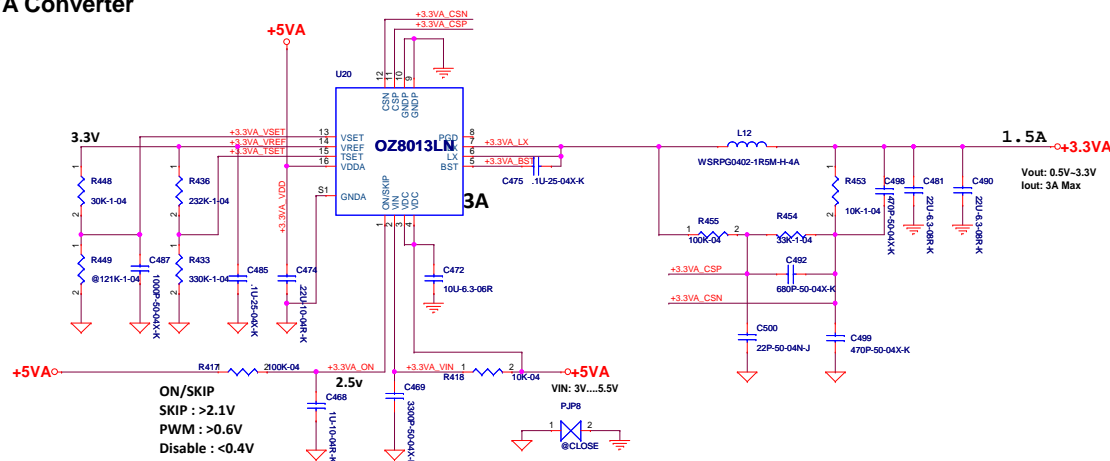
Enhance USB Port



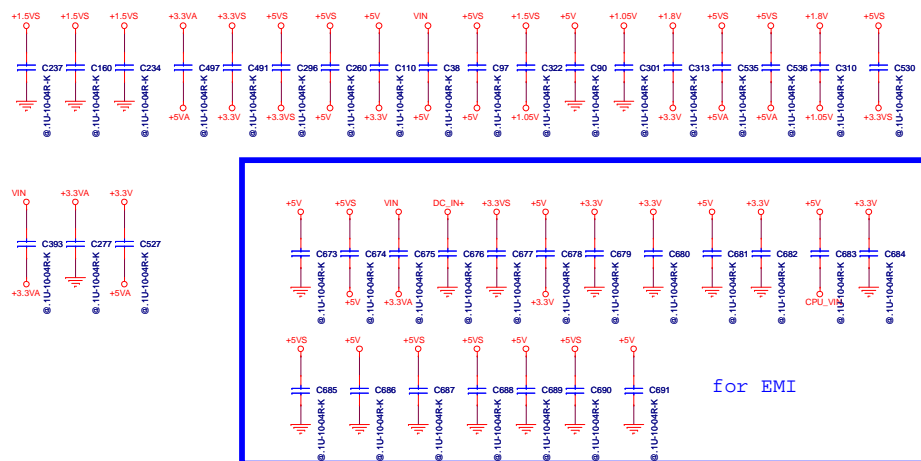
VCCSW



3.3VA Converter

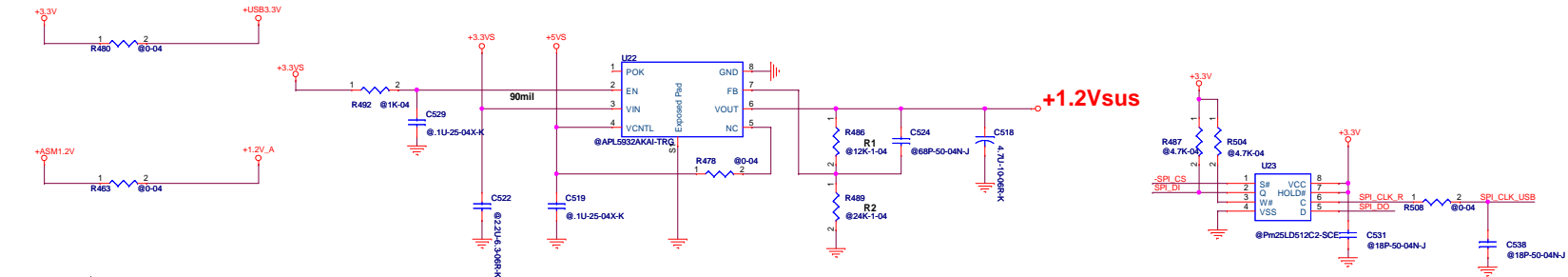


HIGH-SPEED CAP



| Shuttle Inc | | | |
|-------------|------------------------------|-------|----------|
| NH14CU | | | |
| Title | Document Number | Rev | |
| Size | VCC SW/+3.3VA/HIGH-SPEED CAP | B | |
| Custom | | | |
| Date | Thursday, January 17, 2013 | Sheet | 37 of 40 |

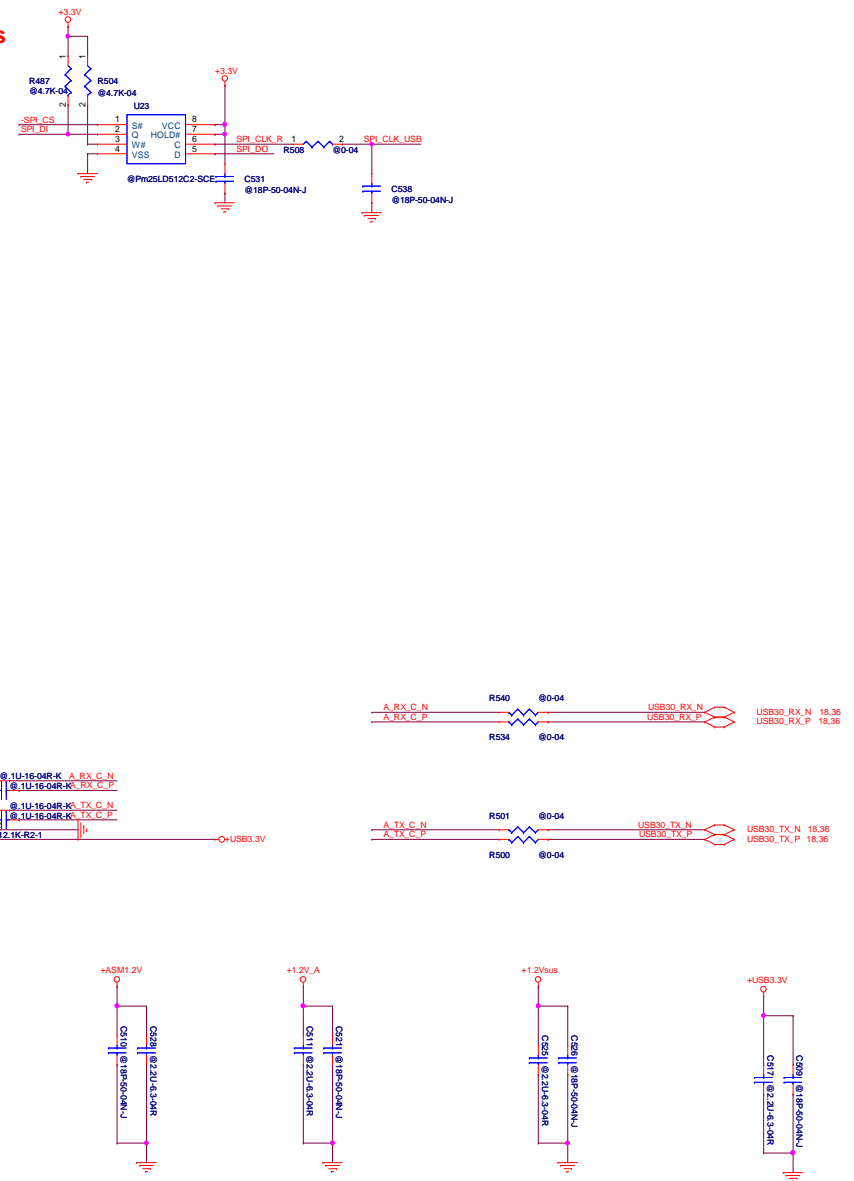
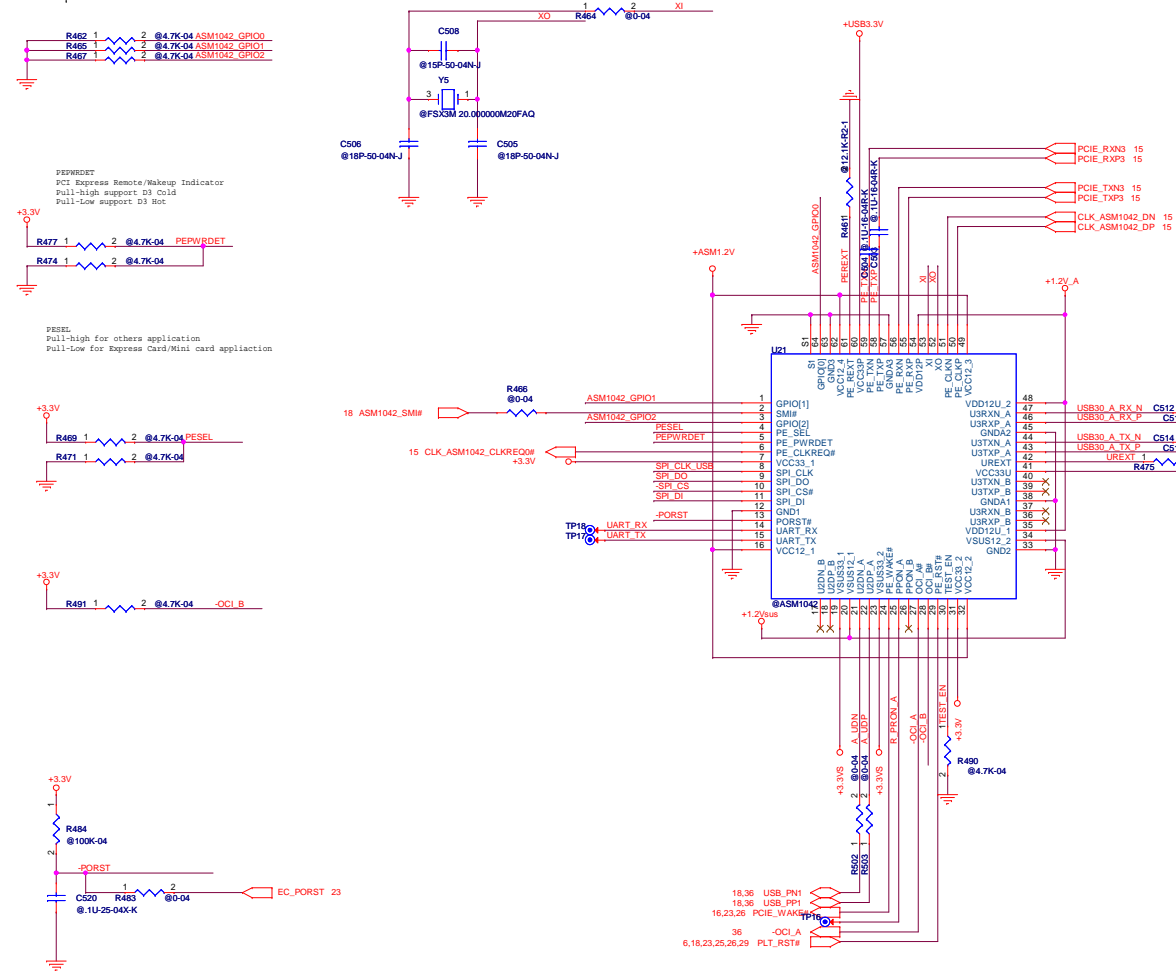
USB 3.0



| GPIO0 | GPIO1 | GPIO2 | Function |
|-------|-------|-------|-----------------------------|
| 1 | 0 | 0 | Synchronous Mode |
| 1 | 1 | 1 | Asynchronous Mode (default) |
| 0 | 0 | x | Debug/Test Mode |

* GPIO0 GPIO1 GPIO2 internal Pull-high

| AS91042 | USB2.0 | USB3.0 |
|---------|-------------|-----------------------------------|
| Sync | 480MHz | 1000MHz from PCIe CLK |
| Async | 20MHz X'tal | 20MHz X'tal (For PCIe over clock) |



MA1:Change net name from PCH_SMB_CLK to PCH_SMB_CLK_DDR
MA2:Change net name from PCH_SMB_DATA to PCH_SMB_DATA_DDR
MA3:DEL CLK_ASM1042_CLKREQ0# path(R87 OP)
MA4:Change ACPRESENT to EC pin 88
MA5:ADD OR FOR 25MHZ CLK(R534)
MA6:ADD OR FOR PCH SATA POWER(B6)
MA7:Sharing System BIOS ROM for KB & EC Codes(Del U7)
MA8:ADD EC_HSCK path for sharing ROM(ADD R540)
MA9:ADD EC_HSCS0# path for sharing ROM(ADD R484)
MA10:ADD EC_HMOSI path for sharing ROM(ADD R212)
MA11:ADD EC_HMISO path for sharing ROM(ADD R482)
MA12:ADD OR FOR AMP_GND(ADD AB12)
MA13:Change CN16 PIN DEFINE
MA14:DEL R147 for PROCHOT issue
MA15:ADD ISEN1 Pull Hi +5V(ADD R356)
MA16:Change C203 SMD CAP TO DIP CAP
MA17:ADD ASM1042_SMI# path(ADD R683)
MA18:Change CN19 PIN DEFINE
MA19:ADD EMI solution(ADD C251,C257,C357,C341,C684,C686,C25,C660,C677 DEL C99,C430)

MB1:Change CPURST# path(OP:R457,Q72,R656,Q71,R659 ADD:R452,R453)
MB2:Change DDR3_DRAMRST_R path(OP:Q67 ADD:R628)
MB3:Change PM_SYSRST# Pull_up power to +3.3V
MB4:Change USB part 1(External USB)to USB part 12 for testingSignal
MB5:Sharing System BIOS ROM for KB & EC Codes(OP:R110,R531,R107,R94)
MB6:ADD SYS_TEMP EC Pin68 for Thermal(ADD RT1,R426)
MB7:ADD CPU Thermal Sensor NTC7717U for Thermal(ADD U27,R693,C887)
MB8:Change SATA3RBIAS external pull-down resistor for testingSignal (R90:1K-1-04)
MB9:ADD RS-232 CONNECT FOR DA18(OP:CN6,,R539,R474,R666,R658,R689,C882,C883,C884,C885)
MB10:Change ASM1042_SMI# path for AMI(GPIO4)

B PHASE

- 1.Page 35 :C187 Modify 0603 to 0402 SIZE
- 2.Page 15,Modify PCIE port4 colay,USB3.0 IC use PORT4 ,add C984,C985,ADD R730,R731,R732,R733
- 3.PAGE 35,REV.B, ADD R131,C199
- 4. Page14, Modify C148,C150 from 15p to 12p
- 5. Page32, Modify 0.75v_DDR power plane
- 6. Page32, REV.B ADD BY-PASS CAPCITOR C731